144/430 MHz, FM MULTI BANDER

TM-742 A/E

144/430/1200 MHz FM TRIBANDER

TM-942 A

SERVICE MANUAL

KENWOOD

B51-8192-00 (B) 1094

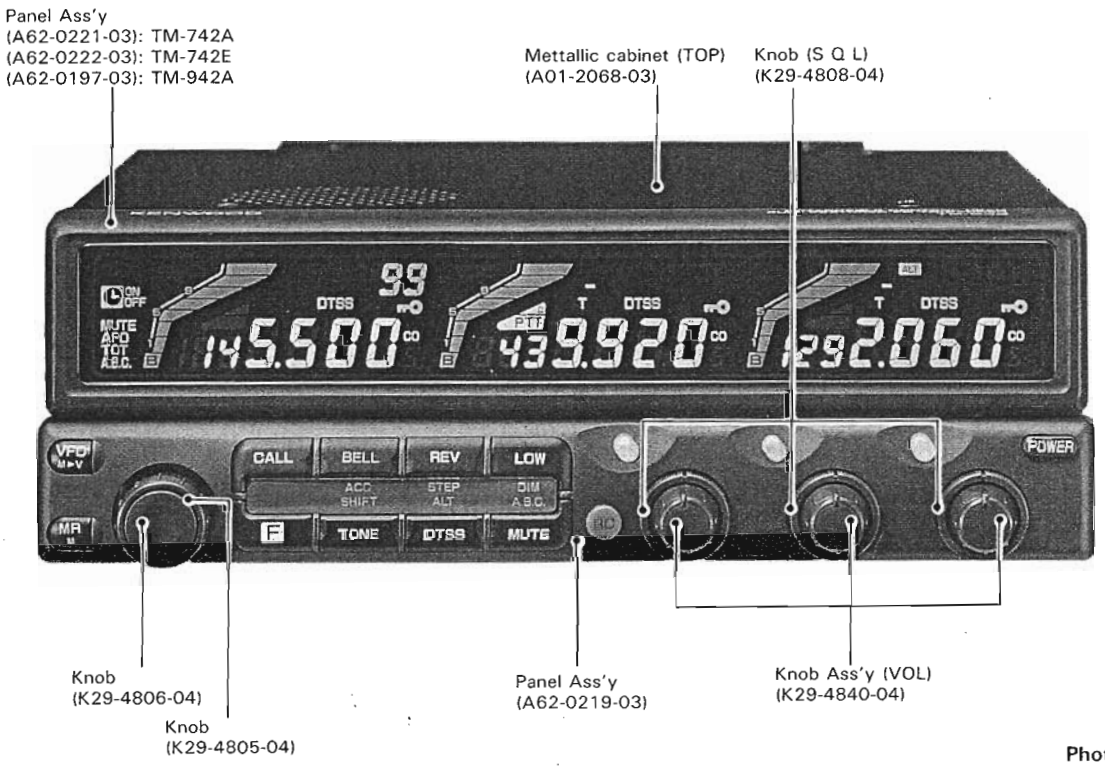


Photo is TM-942A

CONTENTS

OVERVIEW

List of Destinations

Model	Destination	Destination code
TM-742A	North America	K
TM-742A	Canada	P
TM-742E	Europe	E
TM-742E	Europe	E2
TM-742E	Europe	E3
TM-742A	Other countries	M
TM-742A	Other countries	M2

Model	Destination	Destination code
TM-942A	North America	K
TM-942A	Canada	P
TM-942A	Other countries	M

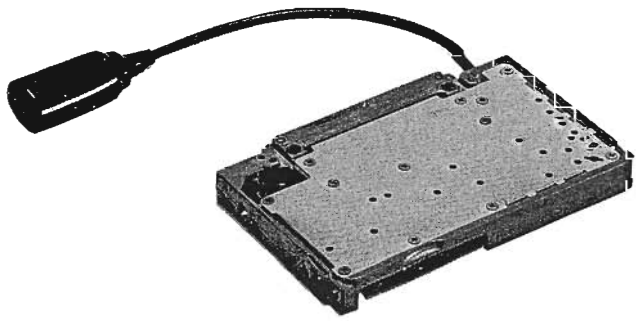
Units for Each Model and Destination

Unit Name	Parts. No.	TM-742A/E							TM-942A			Band Units			
												UT-28S	UT-50S	UT-220S	UT-1200
		K	P	E	E2	E3	M	M2	K	P	M	M (50)	M (50)	K (50)	M (10)
Control Unit	X53-3460-11	○	○						○	○					
Control Unit	X53-3460-21						○				○				
Control Unit	X53-3460-22							○							
Control Unit	X53-3462-71			○		○									
Control Unit	X53-3462-72				○										
Display Unit	X54-3130-11	○	○	○	○	○	○	○	○	○	○				
28TX-RX	X57-3790-01											○			
50TX-RX	X57-3800-01												○		
144TX-RX	X57-3580-11								○	○	○				
144TX-RX	X57-3580-12	○	○	○	○	○	○	○							
220TX-RX	X57-3810-10													○	
440TX-RX	X57-3590-12	○	○								○				
430TX-RX	X57-3590-22						○	○							
430TX-RX	X57-3592-72			○	○	○			○	○					
1200TX-RX	X57-3600-11								○	○	○				○

BAND UNITS

Any of the following optional band units may be installed in the TM-742A/742E.
The same instructions apply for the Tri-Bander as for the Dual-bander.

	OPTIONAL BAND UNIT
TM-742A U.S.A. Version	UT-28S UT-50S UT-220S UT-1200
TM-742A	UT-28S UT-50S UT-1200
TM-742E	UT-28S UT-50S UT-1200



CIRCUIT DESCRIPTION

UT-28S

28 TX-RX Unit Frequency Configuration

The 28 MHz unit incorporates a variable frequency oscillator (VFO), based on a phase-locked-loop (PLL) synthesizer system, that allows a channel step of 5, 10, 15, 20, or 25 kHz to be selected. The frequency in the receive signal channel is mixed with a first local oscillation frequency of 36.83-38.525 MHz to produce a first intermediate frequency (IF) of 8.83 MHz.

This frequency is then mixed with a second local oscillation frequency of 9.285 MHz to produce a second IF of 455 kHz. This is called a double-conversion system. The signal in the transmission channel is produced by direct oscillation, is frequency-divided by a PLL circuit, amplified by a linear amplifier, then transmitted.

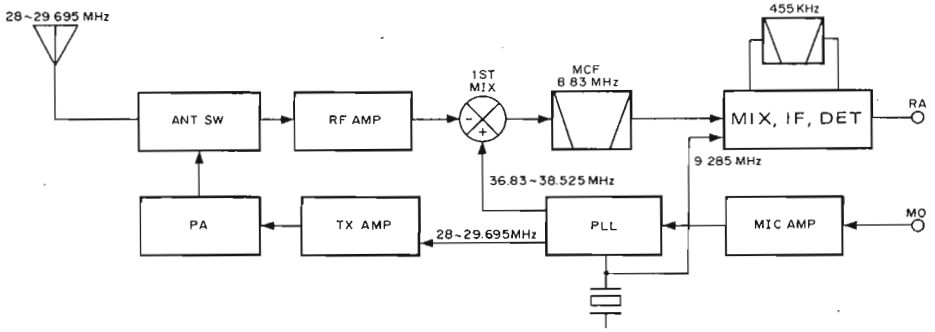


Fig. 1 Frequency configuration

28 TX-RX Unit Receive Signal Channel

- **Outline**

The received signal from the antenna passes through a low-pass filter in the final transmission stage and then through a transmission/reception selection diode switch to the receiving front end. The signal then passes through an antenna matching coil and is amplified to high frequencies by a MOS field-effect transistor. The unwanted components of the signal are eliminated by a bandpass filter consisting of a three-stage variable capacitor. The resulting signal goes to the first mixer, is mixed with the first local signal from the PLL circuit, then converted to the first IF of 8.83 MHz. The unwanted near-by signal components are then eliminated by a two-stage MCF.

The first IF signal is amplified and input to FM IF HIC IC6 (KCD04). This signal is then mixed with the second local oscillation frequency of 9.285 MHz to produce the second IF signal of 455 kHz. The unwanted near-by signal components are then eliminated by an FM ceramic filter. The resulting signal is input to IC6 again, amplified to the second IF signal, and detected to produce an audio signal.

- **Signal-strength meter**

The signal-strength meter output voltage of FM IF HIC IC6 (KCD04) is supplied to the control unit.

Item	Rating
Center frequency (fo)	8830 kHz
Pass bandwidth	± 6 kHz or more at 3 dB
Attenuation bandwidth	± 20 kHz or less at 40 dB ±40 kHz or less at 60 dB
Guaranteed attenuation	70 dB or more within Fo ± 1 MHz (Spurious: 40 dB or more)
Ripple	1 dB or less
Insertion loss	2 dB or less
Terminating impedance	4.7 kΩ//0pF

Table 1 MCF (L71-0422-05) (28TX-RX unit XF1)

Item	Rating
Nominal center frequency	455KHz
6 dB bandwidth	± 6 kHz or more (from 455 kHz)
50 dB bandwidth	± 12.5 kHz or less (from 455 kHz)
Ripple (within ± 5 kHz of 455 kHz	3 dB or less
Insertion loss (at maximum output point)	6 dB or less
Guaranteed attenuation (within ± 100 kHz of 455 kHz)	35 dB or more
I/O matcing impedance	2.0kΩ

Table 2 Ceramic filter CFWM455F (L72-0372-05) (28TX-RX unit CF1)

CIRCUIT DESCRIPTION

- **Shift-register circuit**
  The ES, CK, and DT serial data from the control unit are sent to C1 (BU4094BF) to perform the control operation outlined in the following table:

Pin No.	Name	Function	Pin No.	Name	Function
1	Strobe	Enable input	9	Qs	
2	Data	Serial data input	10	Q's	
3	Clock	Clock input	11	Q8	TX/RX selection. High when TX is set.
4	Q1	TX/RX selection. Low when TX is set	12	Q7	ATT switching: High when ATT is on
5	Q2	TX power selection. Low when middle and low. "H" when high.	13	Q6	High for AM; low for FM; High for narrow; low for wide
6	Q3	TX power selection. Low when high and low. "H" when middle.	14	Q5	High when off band
7	Q4	Low when off band	15	OE	8V
8	Vss	GND	16	VDD	8V

Table 3

- **ATT circuit**
  If there is cross modulation, the ATT circuit operates to attenuate the received signal before it enters Q2 (FET for high-frequency amplification).

28 TX-RX Unit Transmit Signal Channel

- **Outline**
  In the transmission channel, the desired frequency is produced by direct oscillation, and is directly frequency modulated by means of a varicap diode.

- **Modulator circuit**
  The audio signal from the control unit is input to microphone amplifier HIC IC3 (KCA04). IC4 consists of a preemphasis circuit, amplifier, limiter, and splatter circuit that eliminates unwanted high-frequency components. The voltage-controlled oscillator (VFO) signal is directly frequency modulated by means of a varicap diode in the frequency modulator circuit.

- **Younger-stage circuit**
  The signal output from the VCO is input to drive circuit HIC IC16 (KCB16). The amplifier can obtain a stable drive output without adjustment because it has a large bandwidth. An APC circuit controls the collector voltage in the Younger final stage.

- **Power amplifier circuit**
  The drive signal is amplified to the specified level by a discrete transistor. Q2 performs class B amplification, and the collector output voltage is controlled by an APC circuit. Q202 amplifies the power by class C operation, improving the efficiency of the final stage.

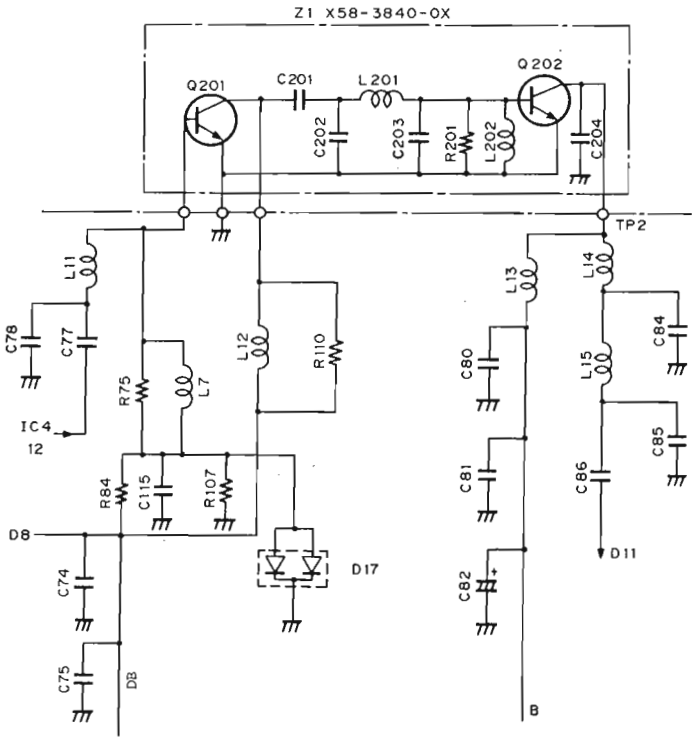


Fig. 2 Power amplifier circuit

CIRCUIT DESCRIPTION

- **APC circuit**

The automatic transmission output control circuit (APC) detects and partially amplifies the power amplifier output with a diode, and controls the output control voltage. The control voltage is output in inverse proportion to the output, so the control voltage output is always constant. To protect the radio against excessive temperature rise, the high-power unit has a thermal switch. The high-power unit is automatically set to a low power by the thermal switch if it exceeds the specified temperature.

- **8T (8 V during transmission) and unlock signal**

The signal output from pin 4 of IC1 is high during reception, Q13 is turned on, and Q14 and Q11 are turned off. No voltage appears at the collector (8T) of Q11. Serial data is output from the control unit during transmission and input to shift register IC1. Pin 4 of IC1 is then made low. Therefore, Q13 is turned off, and 14 and Q11 are turned on. An 8 V voltage is applied to the collector (8T) of Q11.

If the PLL circuit is unlocked during transmission, the LD pin goes low, Q24 is turned off, Q13 is turned on, Q14 is turned off, Q11 for 8T switching control is turned off, and the 8T line does not operate.

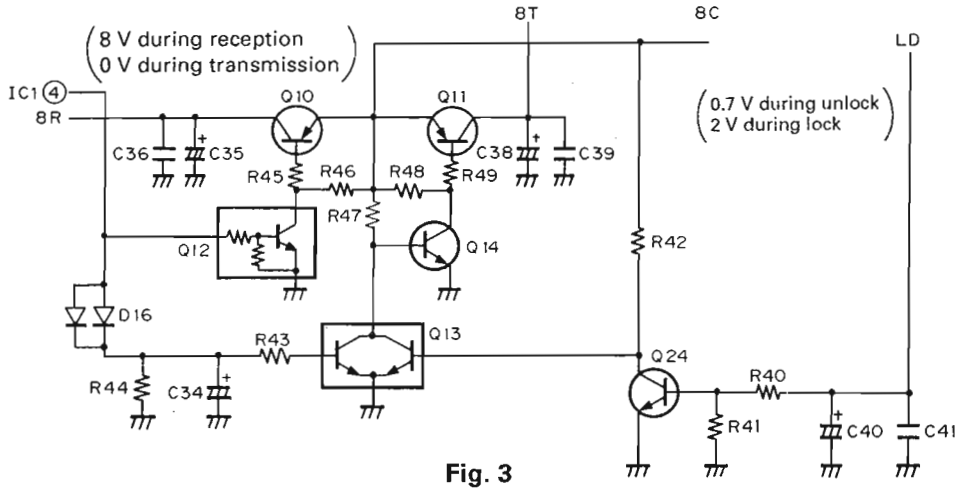


Fig. 3

28 TX-RX Unit PLL Synthesizer

The VCO and PLL circuits are housed in a solid shielding case as a hybrid integrated circuit. Comparison frequencies are produced by dividing a 9.285 MHz reference oscillation frequency by 1857 to correspond to the 5, 10, 15, 20, and 25 kHz channel steps.

For 28 MHz, the relationship between f_{VCO} (RX) and each frequency division ratio is given by

$f_{VCO} = (28+8.83)=\{(nx64)+A\}xf_{osc}/R$

Where: f_{VCO}=VCO output frequency

n: Binary 10-bit programmable counter setting value

A: Binary 6-bit programmable counter setting value

f_{osc}: Reference oscillation frequency of 9.285 MHz

R: Binary 16-bit programmable counter setting value 1857

In this case, n is 155, and A is 6.

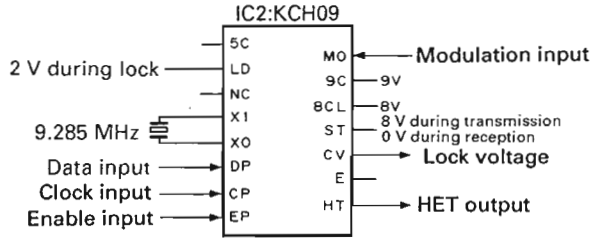


Fig. 4

Therefore, f_{VCO} ={(115x64)+6}x9285/1857
=(7360+6)x5
=36.83 MHz

The following table lists the pin functions of the PLL circuit:

Pin name	Function	Pin name	Function
5C	5V	MO	Modulation signal input
LD	Lock signal (2 V during locking)	9c	9v
NC	Unused	8CL	8 V (ripple filter)
XI XO	9.285 MHz crystal oscillation	ST	8 V during transmission; 0 V during reception
		CV	Lock voltage output
DP	Data input	E	GND
CP	Clock input	HT	HET output
EP	Enable input		

Table 4 PLL circuit pin functions

CIRCUIT DESCRIPTION

UT-50S

50 TX-RX Unit Frequency Configuration

The 50 MHz unit incorporates a variable frequency oscillator (VFO), based on a phase-locked-loop (PLL) synthesizer system, that allows a channel step of 5, 10, 15, 20, or 25 kHz to be selected. The frequency in the receive signal channel is mixed with a first local oscillation frequency of 60.595-64.590 MHz to produce a first intermediate frequency (IF) of 10.595 MHz. This frequency is then mixed with a second local oscillation frequency of 11.05 MHz to produce a second IF of 455 kHz. This is called a double-conversion system. The signal in the transmission channel is produced by direct oscillation, and is frequency-divided by a PLL circuit, amplified by a linear amplifier, then transmitted.

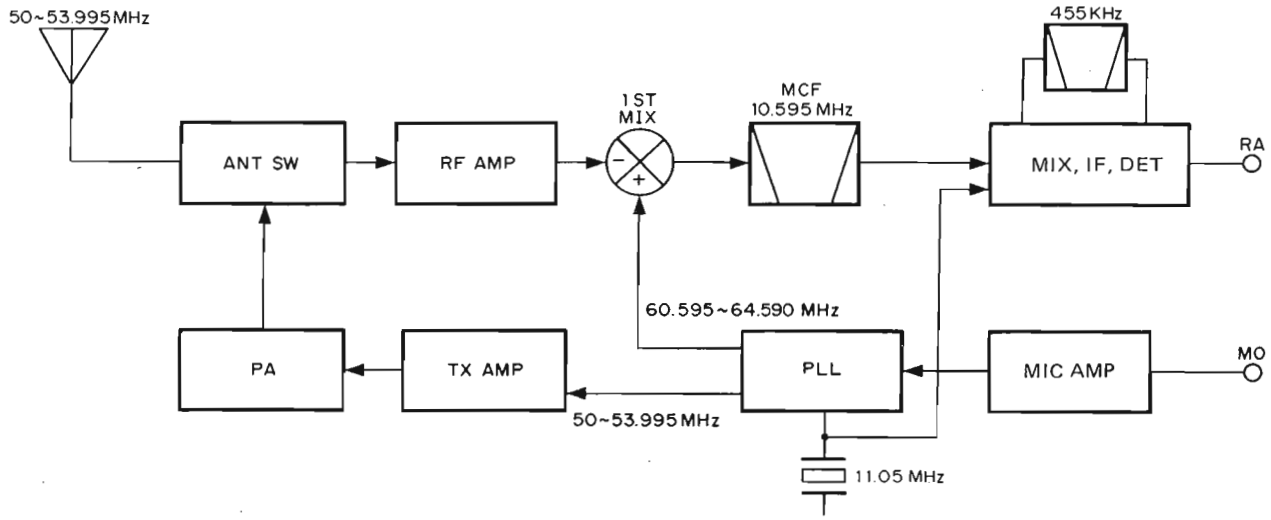


Fig. 5 Frequency Configuration

50 TX-RX Unit Receive Signal Channel

- **Outline**

The received signal by the antenna passes through a low-pass filter in the final transmission stage and then through a transmission/reception selection diode switch to the receiving front end. The signal then passes through an antenna matching coil and is amplified to high frequencies by a GaAs (gallium arsenide) field-effect transistor. The unwanted components of the signal are eliminated by a bandpass filter consisting of a three-stage variable capacitor. The resulting signal goes to the first mixer, is mixed with the first local signal from the PLL circuit, then converted to the first IF of 10.595 MHz.

Item	Rating
Center frequency	10.595 MHz
Pass bandwidth	±6.5 kHz or more at 3 dB
Attenuation bandwidth	±23 kHz or less at 40 dB ±40 kHz or less at 60 dB
Guaranteed attenuation	70 dB or more within Fo ±1 MHz (Spurious: 40 dB or more)
Ripple	1 dB or less
Insertion loss	1.5 dB or less
Terminating impedance	2.9 kΩ//0pF

Table 5 MCF (L71-0421-05) (50TX-RX unit XF1)

The unwanted near-by signal components are then eliminated by a two-stage MCF.

The first IF signal is amplified and input to FM IF HIC IC6 (KCD04). This signal is then mixed with the second local oscillation frequency of 11.05 MHz to produce the second IF signal of 455 kHz. The unwanted near-by signal components are then eliminated by an FM ceramic filter. The resulting signal is input to IC6 again, amplified to the second IF signal, and detected to produce an audio signal.

Item	Rating
Nominal center frequency	455KHz
6 dB bandwidth	±6.0 kHz or more (from 455 kHz)
50 dB bandwidth	±12.5 kHz or less (from 455 kHz)
Ripple (within ±5 kHz of 3455 kHz)	3 dB or less
Insertion loss (at maximum output point)	6 dB or less
Guaranteed attenuation (within ±100 kHz of 455 kHz)	35 dB or more
Terminating impedance	2.0 kΩ

Table 6 Ceramic filter CFWM455F (L72-0372-05) (50TX-RX unit CF1)

CIRCUIT DESCRIPTION

● Signal-strength meter

The signal-strength meter output voltage of FM IF HIC IC6 (KCD04) is supplied to the control unit.

● Shift-register circuit

The ES, CK, and DT serial data from the control unit are sent to IC1 (BU4094BF) to perform the control operation outlined in the following table:

Pin No.	Name	Function	Pin No.	Name	Function
1	Strobe	Enable input	9	Qs	
2	Data	Serial data input	10	Q's	
3	Clock	Clock input	11	Q8	TX/RX selection. High when TX is set.
4	Q1	TX/RX selection. Low when TX is set	12	Q7	ATT switching: High when ATT is on
5	Q2	TX power selection. Low when middle and low. "H" when high.	13	Q6	High for AM; low for FM
6	Q3	TX power selection. Low when high and low. "H" when middle.	14	Q5	High when off band
7	Q4	Low when off band	15	OE	8V
8	Vss	GND	16	VDD	8V

Table 7

● ATT circuit

If there is cross modulation, the ATT circuit operates to attenuate the received signal before it enters Q2 (FET for high-frequency amplification).

50 TX-RX Unit Transmit Signal Channel

● Outline

In the transmission channel, the desired frequency is produced by direct oscillation, and is directly frequency modulated by means of a varicap diode.

● Modulator circuit

The audio signal from the control unit is input to microphone amplifier HIC IC3 (KCA04). IC4 consists of a preemphasis circuit, amplifier, limiter, and splatter circuit that eliminates unwanted high-frequency components. The voltage-controlled oscillator (VFO) signal is directly frequency modulated by means of a varicap diode in the frequency modulator circuit.

● Younger-stage circuit

The signal output from the VCO is input to drive circuit HIC IC4 (KCB18). The amplifier can obtain a stable drive output without adjustment because it has a large bandwidth. An APC circuit controls the collector voltage in the Younger final stage.

● Power amplifier circuit

The drive signal is amplified to the specified level by a discrete transistor. Q201 performs class B amplification, and the collector output voltage is controlled by an APC circuit. Q202 amplifies the power by class C operation, improving the efficiency of the final stage.

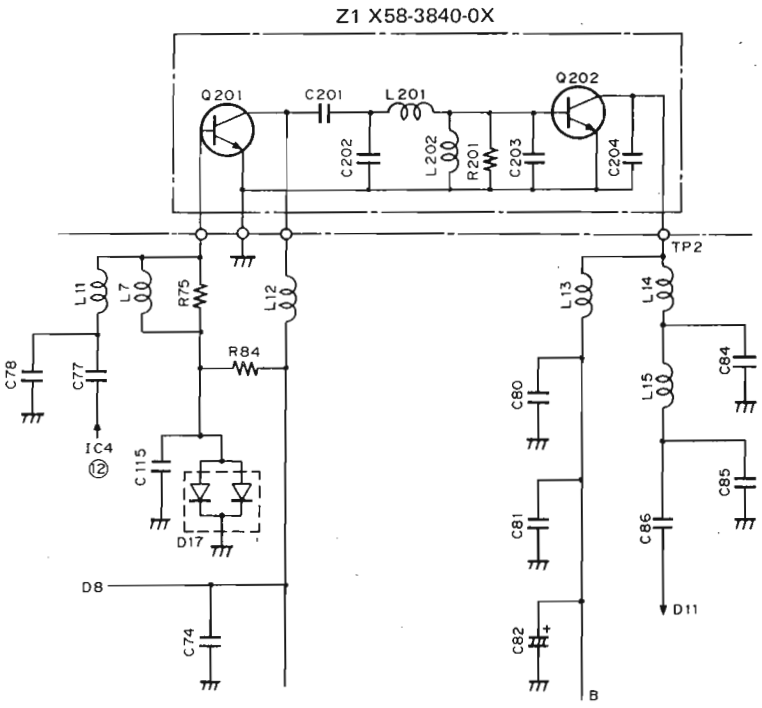


Fig. 6 Power amplifier circuit

CIRCUIT DESCRIPTION

- **APC circuit**

The automatic transmission output control circuit (APC) detects and partially amplifies the power amplifier output with a diode, and controls the output control voltage. The control voltage is output in inverse proportion to the output, so the control voltage output is always constant. To protect the radio against excessive temperature rise, the high-power unit has a thermal switch. The high-power unit is automatically set to a low power by the thermal switch if it exceeds the specified temperature.

- **LPF circuit**

The low-pass filter sets the pole to the second and third harmonics, and cuts the frequency, by having the polar Chebyshev characteristics. To cut high frequencies, a filter with Chebyshev characteristics is used before the antenna.

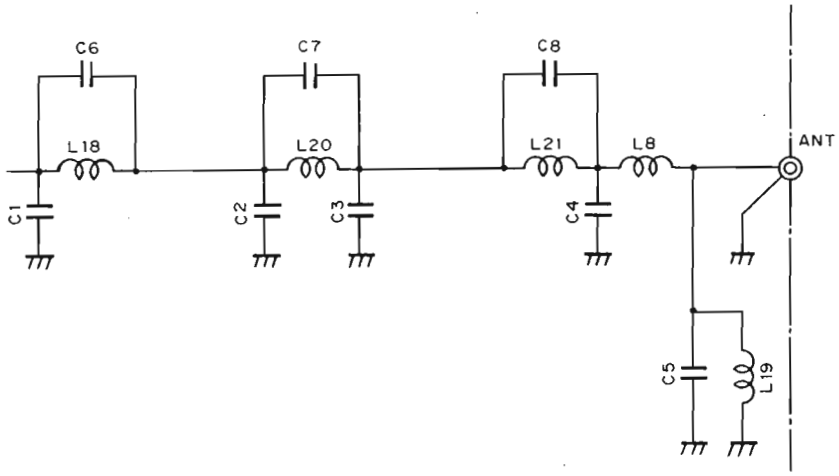


Fig. 7 LPF Circuit

- **8T (8 V during transmission) and unlock signal**

The signal output from pin 4 of IC1 is high during reception, Q13 is turned on, and Q14 and Q11 are turned off. No voltage appears at the collector (8T) of Q11. Serial data is output from the control unit during transmission and input to shift register IC1. Pin 4 of IC1 is then made low. Therefore, Q13 is turned off, Q14 and Q11 are turned on. An 8 V voltage is applied to the collector (8T) of Q11.

If the PLL circuit is unlocked during transmission, the LD pin goes low, Q24 is turned off, Q13 is turned on, Q14 is turned off, Q11 for 8T switching control is turned off, and the 8T line does not operate.

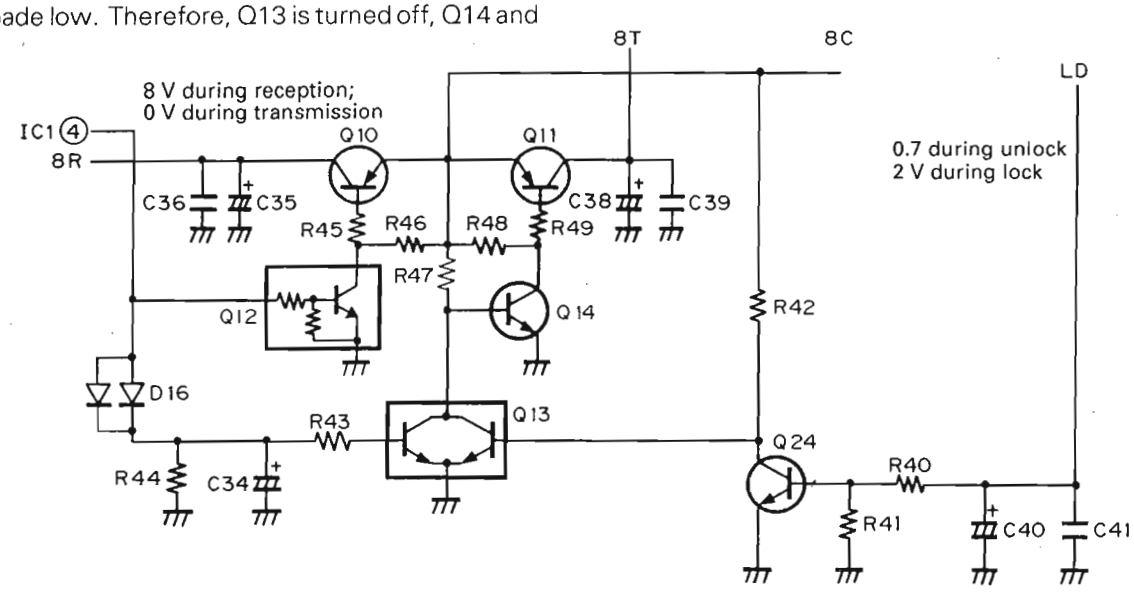


Fig. 8

CIRCUIT DESCRIPTION

- **50 TX-RX Unit PLL Synthesizer**

The VCO and PLL circuits are housed in a solid shielding case as a hybrid integrated circuit. Comparison frequencies are produced by dividing a 11.05 MHz reference oscillation frequency by 2210 to correspond to the 5, 10, 15, 20, and 25 kHz channel steps.

For 50 MHz, the relationship between f_{VCO} (RX) and each frequency division ratio is given by

$f_{VCO}=(50+10.595)=\{(nx64)+A\}xf_{osc}/R$

Where: f_{VCO}=VCO output frequency

n: Binary 10-bit programmable counter setting value

A: Binary 6-bit programmable counter setting value

f_{osc}: Reference oscillation frequency of 11.05 MHz

R: Binary 16-bit programmable counter setting value

In this case, n is 189, and A is 23.

Therefore, f_{VCO} $=\{(189x64)+23\}x11050/2210$

$=(12096+23)x5$

$= 60.595$ MHz

The following table lists the pin functions of the PLL circuit:

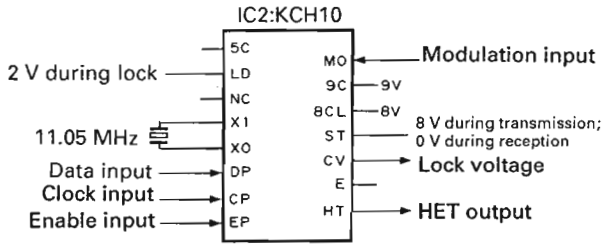


Fig. 9

Pin name	Function	Pin name	Function
5C	5V	MO	Modulation signal input
LD	Lock signal (2 V during locking)	9C	9V
NC	Unused	8CL	8 V (ripple filter)
XI XO	11.05 MHz crystal oscillation	ST	8 V during transmission; 0 V during reception
	Data input	CV	Lock voltage output
DP	Clock input	E	GND
CP	Enable input	HT	HET output
EP			

Table 8 PLL circuit pin functions

CIRCUIT DESCRIPTION

144 TX-RX Unit Frequency Configuration

The 144 MHz unit incorporates a digital variable-frequency oscillator (VFO) that can freely select a channel step of 5, 10, 12.5, 15, 20, or 25 kHz with a Phase-Locked-Loop (PLL) synthesizer system.

The frequency in the receive signal channel is mixed with a first local oscillation frequency of 133.300-137.295 MHz to produce a first intermediate frequency of 10.7 MHz. This frequency is then mixed with a second local oscillation frequency of 10.245 MHz to produce a second intermediate frequency of 455 kHz. This is called a double-conversion system.

The signal in the transmission channel is directly oscillated and frequency-divided by a PLL circuit, amplified by a straight amplifier, then transmitted.

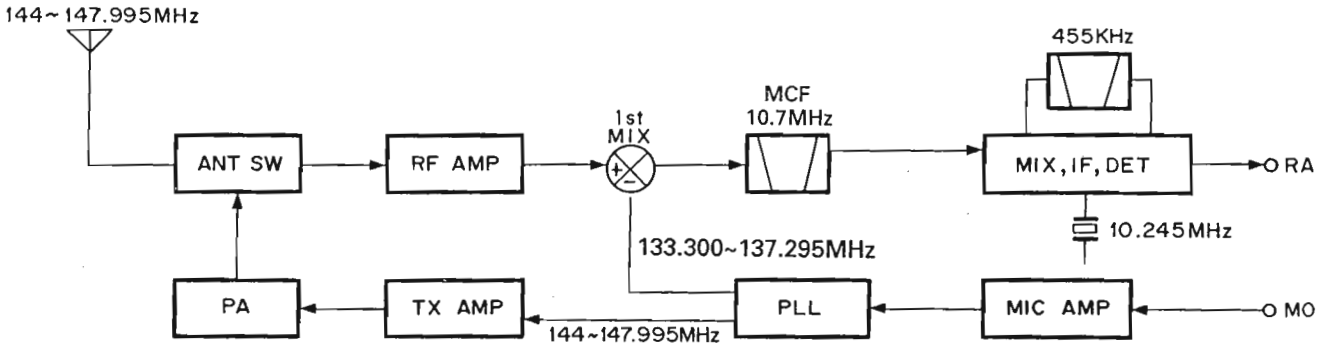


Fig. 10 Frequency configuration

144 TX-RX Unit Receive Signal Channel

- **Outline**

For the 144 MHz unit,the received signal from an antenna is passed through a low-pass filter in the final transmission stage and sent through a transmission/reception selection diode switch to the receiving front end. The signal is then passed through an antenna matching coil and amplified to high frequencies by a GaAs (gallium arsenide) field-effect transistor. The unwanted components of the signal are eliminated by a bandpass filter consisting of a three-stage variable capacitor. The resultant signal is sent to the first mixer, mixed with the first local signal from a PLL circuit, then converted to a first intermediate frequency of 10.7 MHz. The unwanted near-by signal components are then eliminated by a two-stage MCF.

Item	Rating
Nominal center frequency (fo)	10.7MHz
Pass band width	±7.5kHz or less at 3dB
Attenuation band width	±25kHz or less at 40dB ±45kHz or less at 60dB
Ripple	1.0dB or less
Insertion loss	1.5dB or less
Guaranteed attenuation	70dB or more within ±1MHz (Spurious : 40dB or more at fo ~ fo + 500kHz) 80dB or more at fo – (900 – 920kHz)
Terminating impedance	3kΩ/0pF

Table 9 MCF (L71-0228-05) (144 TX-RX unit XF1)

Item	Rating
Nominal center frequency	455kHz ± 1kHz
6dB bandwidth	±6kHz or more (from 455kHz)
50dB bandwidth	±12.5kHz or less (from 455kHz)
Ripple (within ±4kHz of 455kHz)	3dB or less
Insertion loss	6dB or less
Guaranteed attenuation (within ±100kHz of 455kHz)	35dB or more
I/O matching impedance	2.0kΩ

Table 10 Ceramic filter CFWM455F (L72-0372-05) (144 TX-RX unit CF1)

CIRCUIT DESCRIPTION

The first intermediate-frequency signal is amplified and input to FM IF HIC IC5 (KCD04). This signal is then mixed with a second local oscillation frequency of 10.245MHz to produce a second intermediate-frequency signal of 455 kHz. The unwanted near-by signal components are then eliminated by an FM ceramic filter. The resultant signal is input to IC5 again, amplified to a second intermediate-frequency signal, and detected to produce an audio signal.

- **Signal-strength meter**

The signal-strength meter output voltage of FM IF HIC IC5 (KCD04) is supplied to the control unit.

- **Shift-register circuit**

The ES, CK, and DT serial data from the control unit are sent to IC1 (BU4094BF) to perform the control operation outlined in the following table:

Pin NO.	Name	Function	Pin No.	Name	Function
1	Strobe	Enable input	9	Q_S	
2	Data	Serial data input	10	Q'_S	
3	Clock	Clock input	11	Q8	TX/RX selection. "H" when TX is set.
4	Q1	TX/RX selection. "L" when TX is set	12	Q7	439/144 MHz selection. "H" when 144MHz is set.
5	Q2	TX power selection. "L" when middle and low. "H" when high.	13	Q6	
6	Q3	TX power selection. "L" when high and low. "H" when middle.	14	Q5	
7	Q4		15	OE	8V
8	V_{ss}	GND	16	V_{DD}	8V

Table 11

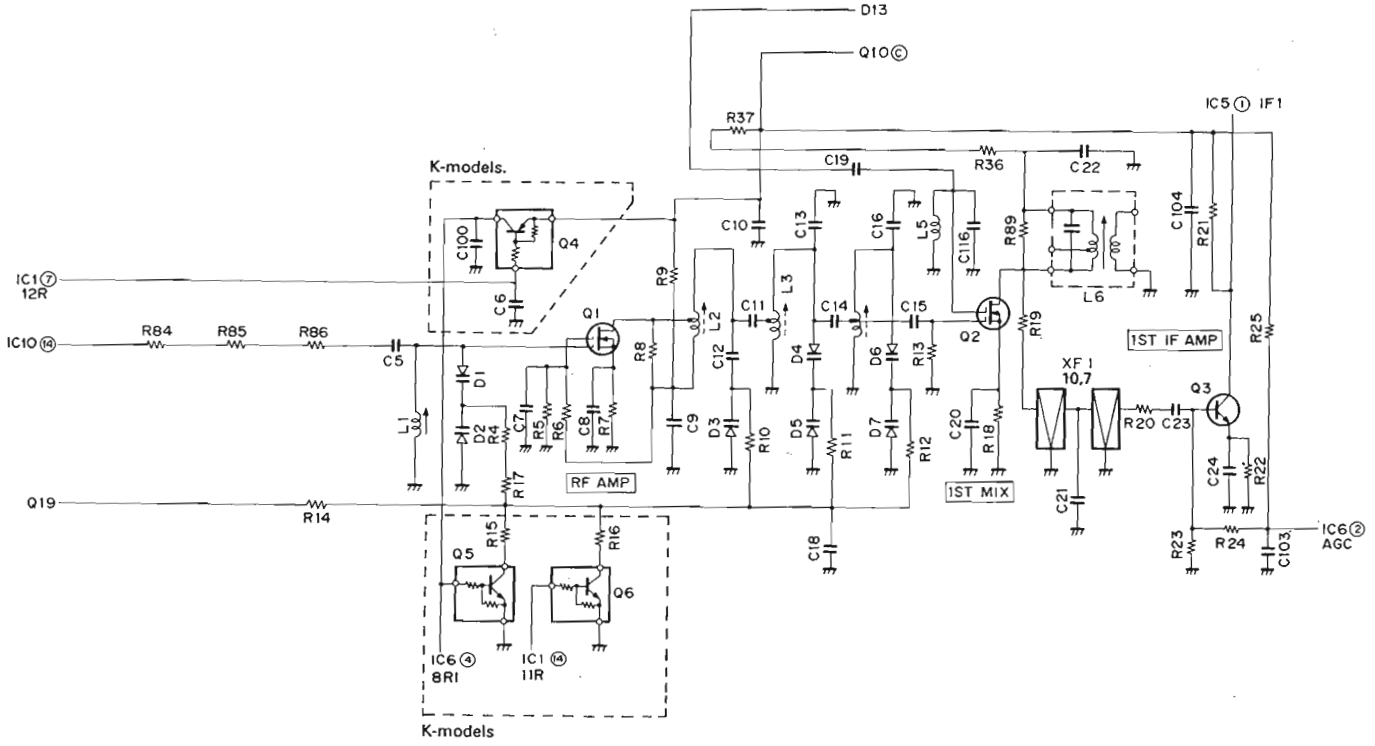


Fig. 11

CIRCUIT DESCRIPTION

144 TX-RX Unit Transmit Signal Channel

- **Outline**

In the transmission channel, the desired frequency is directly oscillated and directly frequency modulated by means of a varicap diode.

- **Modulator circuit**

The audio signal from the control unit is input to microphone amplifier HIC IC7 (KCA04). IC4 consists of a preemphasis circuit, amplifier, limiter, and splatter circuit that eliminate unwanted high-frequency components. The voltage-controlled oscillator (VCO) signal is directly frequency modulated by means of a varicap diode in the frequency modulator circuit.

- **Younger-stage circuit**

The signal output from the VCO is input to drive circuit HIC IC8 (KCB11). The amplifier can obtain a stable drive output without adjustment because it has a wide band. An APC circuit controls the collector voltage in the younger final stage.

- **Power amplifier circuit**

A drive signal is input to power module IC10 and amplified to the specified level.

- **APC circuit**

The automatic transmission output control circuit (APC) detects and partially amplifies the power module output with a diode and controls the output control voltage. The control voltage is output in inverse proportion to the output, so the control voltage output is always constant. To protect the set against excessive temperature rise, the high-power unit has a thermal switch. The high-power unit is automatically set to a low power by the thermal switch when it exceeds the specified temperature.

144 TX-RX Unit PLL Synthesizer

The VCO and PLL circuit are housed in a solid shielding case as a hybrid integrated circuit. Comparison frequencies of 6.25 kHz and 5 kHz are produced by dividing a 12.8 MHz reference oscillation frequency by 2048 and 2560 to correspond to 5, 10, 12.5, 15, 20, and 25 kHz channel steps.

For 144 MHz, the relationship between f_{VCO} (Rx) and each frequency division ratio is given by

$f_{VCO}=(144 - 10.7)= \{(n \times 128) + A\} \times f_{osc} \div R$

Where: f_{VCO}= VCO output frequency

n : Binary 10-bit programmable counter setting value

A : Binary 7-bit programmable counter setting value

f_{osc}: Reference oscillation frequency of 12.8 MHz

R: Binary 14-bit programmable counter setting value 2048

In this case, n is 208, and A is 36.

Therefore, $f_{VCO}= \{(208 \times 128) + 36\} \times 12800 / 2560$

$= \{26624 + 37\} \times 5$

$= 133300$ kHz $= 133.300$ MHz

The following table lists the pin functions of the PLL circuit:

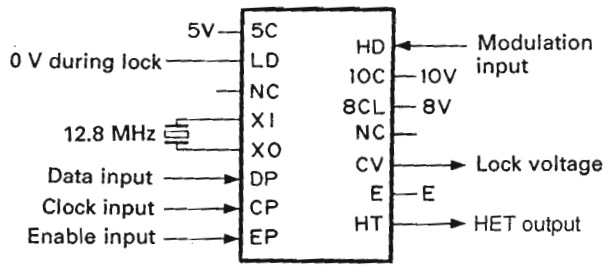


Fig. 12 IC11 KCH05

Pin name	Function	Pin name	Function
5C	5V	MO	Modulation signal input
LD	Lock signal (on during lock)	10C	10V
NC	Unused	8CL	8V (ripple filter)
XI	12.8 MHz crystal oscillation	NC	Unused
XO		CV	Lock voltage output
DP	Data input	E	GND
CP	Clock input	HT	HET output
EP	Enable input		

Table 12

CIRCUIT DESCRIPTION

- **8T (8 V during transmission) and unlock signal**

A 0.7 V voltage is applied to the base of Q13 during reception, Q13 is set on, Q14 is set off, and Q11 is set off. No voltage appears at the collector (8T) of Q11. Serial data is output from the control unit during transmission and input to shift register IC1. Pin 4 of IC1 is then set low. Therefore, Q13 is changed from on to off, Q14 from off to on, and Q11 from off to on. An 8 V voltage is applied to the collector (8T) of Q11.

An unlock circuit is activated only during transmission. The LD signal output from the PLL circuit is ORed with the signal at pin 4 of IC1 using D11 as shown in the figure, so the LD signal is set high during unlock. Therefore, no voltage appears at the collector (8T) of Q11 and no transmission wave is output to the reception state.

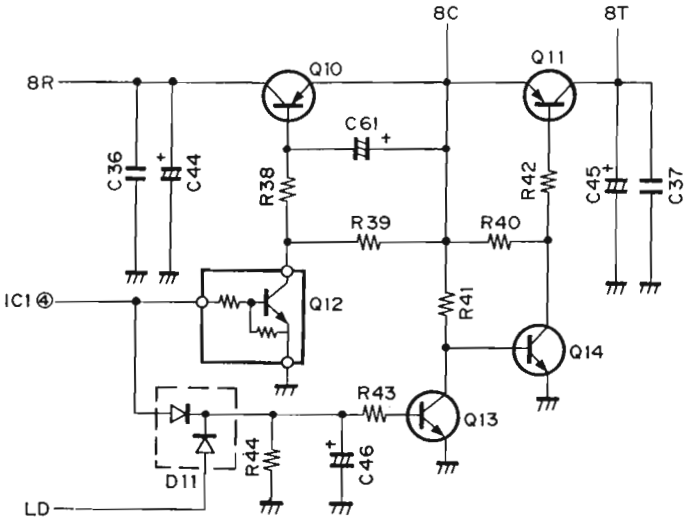


Fig. 13

UT-220S

220 TX-RX Unit Frequency Configuration

The 220 MHz unit incorporates a variable frequency oscillator (VFO), based on a phase-locked-loop (PLL) synthesizer system, that allows a channel step of 5, 10, 12.5, 15, 20, or 25 kHz to be selected. The frequency in the receive signal channel is mixed with a first local oscillation frequency of 189.175-194.17 MHz to produce a first intermediate frequency (IF) of 30.825 MHz. This frequency is then mixed with a second local oscillation frequency of 30.37 MHz to produce a second IF of 455 kHz. This is called a double-conversion system. The signal in the transmission channel is produced by direct oscillation, and is frequency-divided by a PLL circuit, amplified by a linear amplifier, then transmitted.

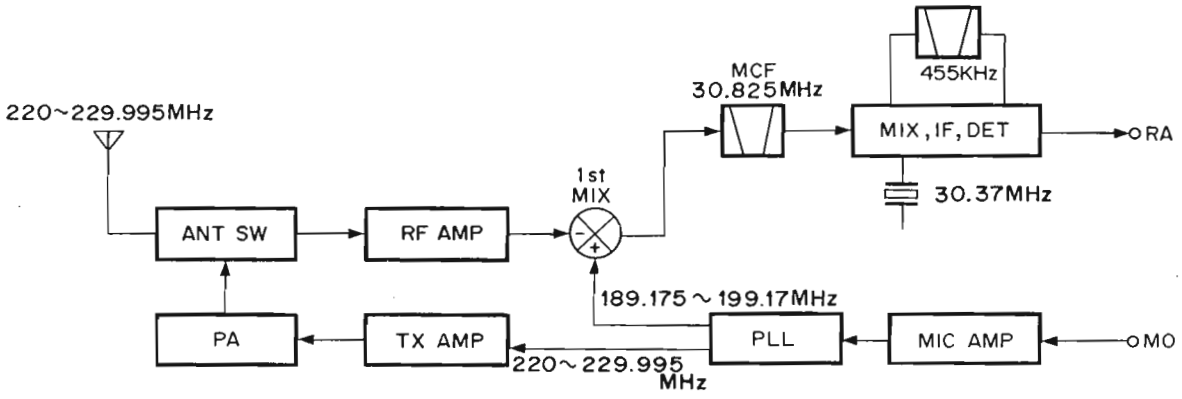


Fig. 14 Frequency configuration

CIRCUIT DESCRIPTION

220 TX-RX Unit Receive Signal Channel

• Outline

The received signal from the antenna passes through a low-pass filter in the final transmission stage and then through a transmission/reception selection diode switch to the receiving front end. The signal then passes through an antenna matching coil and is amplified to high frequencies by a GaAs (gallium arsenide) field-effect transistor. The unwanted components of the signal are eliminated by a bandpass filter consisting of a three-stage variable capacitor. The resulting signal goes to the first mixer (GaAs field-effect transistor), is mixed with the first local signal from the PLL circuit, then converted to a first If of 30.825 MHz. The unwanted near-by signal components are then eliminated by a two-stage MCF.

The first IF signal is amplified and input to FM IF HIC IC5 (KCD04). This signal is then mixed with the second local oscillation frequency of 30.37 MHz to produce the second IF signal of 455 kHz. The unwanted near-by signal components are then eliminated by an FM ceramic filter. The resulting signal is input to IC5 again, amplified to the second IF signal, and detected to produce an audio signal.

Item	Rating
Center frequency (fo)	30,825 MHz
Pass bandwidth	± 7.5 kHz or more at 3 dB
Attenuation bandwidth	± 28 kHz or less at 40 dB
Guaranteed attenuation	60 dB or more within Fo ± 1 MHz (Spurious: 40 dB or more)
Ripple	1.5 dB or less
Insertion loss	3 dB or less
Terminating impedance	4.7 kΩ//0pF

Table 13 MCF (L71-0420-05) (220 TX-RX unit XF1)

Item	Rating
Nominal center frequency	455KHz
6 dB bandwidth	± 6 kHz or more (from 455 kHz)
50 dB bandwidth	± 12.5 kHz or less (from 455 kHz)
Ripple (within ± 5 kHz of 455 kHz)	3 dB or less
Insertion loss (at maximum output point)	6 dB or less
Guaranteed attenuation (within ± 100 kHz of 455 kHz)	35 dB or more
I/O matcing impedance	2.0kΩ

Table 14 Ceramic filter CFWM455F (L72-0372-05) (220TX-RX unit CF1)

• Signal-strength meter

The signal-strength meter output voltage of FM IF HIC IC5 (KCD04) is supplied to the control unit.

• Shift-register circuit

The ES, CK, and DT serial data from the control unit are sent toIC1 (BU4094BF) to perform the control operation outlined in the following table:

Pin No.	Name	Function
1	Strobe	Enable input
2	Data	Serial data input
3	Clock	Clock input
4	Q1	TX/RX selection. Low when TX is set.
5	Q2	TX power selection. Low when middle and low. High when high.
6	Q3	TX power selection. Low when high and low. High when middle.
7	Q4	
9	Q3	
10	Q3	
11	Q8	
12	Q7	
13	Q6	
14	Q5	
15	QE	8V

Table 15

CIRCUIT DESCRIPTION

220 TX-RX Unit Transmit Signal Channel

- **Outline**

In the transmission channel, the desired frequency is produced by direct oscillation, and is directly frequency modulated by means of a varicap diode.

- **Modulator circuit**

The audio signal from the control unit is input to microphone amplifier HIC IC7 (KCA04). IC4 consists of a preemphasis circuit, amplifier, limiter, and splatter circuit that eliminates unwanted high-frequency components. The voltage-controlled oscillator (VFO) signal is directly frequency modulated by means of a varicap diode in the frequency modulator circuit.

- **Younger-stage circuit**

The signal output from the VCO is input to drive circuit HIC IC8 (KCB15). The amplifier can obtain a stable drive output without adjustment because it has a large bandwidth. An APC circuit controls the collector voltage in the Younger final stage.

- **Power amplifier circuit**

The drive signal is input to power module IC10 and amplified to the specified level.

220 TX-RX Unit PLL Synthesizer

The VCO and PLL circuits are housed in a solid shielding case as a hybrid integrated circuit. Comparison frequencies are produced by dividing a 12.8 MHz reference oscillation frequency by 2248 and 2560 to correspond to the 5, 10, 12.5, 15, 20, and 25 kHz channel steps.

For 220 MHz, the relationship between f_{VCO} (RX) and each frequency division ratio is given by

$f_{VCO}=(220+30.825)=\{(nx128)+A\}xf_{osc}/R$

Where: f_{VCO}=VCO output frequency

n: Binary 10-bit programmable counter setting value

A: Binary 7-bit programmable counter setting value

f_{osc}: Reference oscillation frequency of 12.8 MHz

R: Binary 10-bit programmable counter setting value 2560

In this case, n is 295, and A is 75.

Therefore, f_{VCO} $=\{(295x128)+75\}x12800/2560$
$=(33760+75)x5$
$=189.175$ MHz

The following table lists the pin functions of the PLL circuit:

- **APC circuit**

The automatic transmission output control circuit (APC) detects and partially amplifies the power amplifier output with a diode and controls the output control voltage. The control voltage is output in inverse proportion to the output, so the control voltage output is always constant.

- **8T (8 V during transmission) and unlock signal**

A 0.7 V voltage is applied to the base of Q13 during reception, Q13 is turned on, and Q14 and Q11 are turned off. No voltage appears at the collector (8T) of Q11. Serial data is output from the control unit during transmission and input to shift register IC1. Pin 4 of IC1 is then made low. Therefore, Q13 is turned off, and Q14 and Q11 are turned on. An 8 V voltage is applied to the collector (8T) of Q11.

The unlock circuit is activated only during transmission. The LD pin signal output from the PLL circuit is ORed with the signal at pin 4 of IC1 using D11, as shown in the figure, so the LD signal is made high during unlock. Therefore, no voltage appears at the collector (8T) of Q11, and no transmission signal is output during reception.

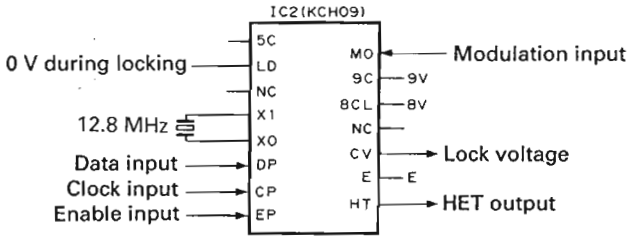


Fig. 15

Pin name	Function	Pin name	Function
5C	5V	MO	Modulation signal input
LD	Lock signal (0 V during locking)	9C	9V
NC	Unused	8CL	8 V (ripple filter)
XI XO	12.8 MHz crystal oscillation	NC	
		CV	Lock voltage output
DP	Data input	E	GND
CP	Clock input	HT	HET output
EP	Enable input		

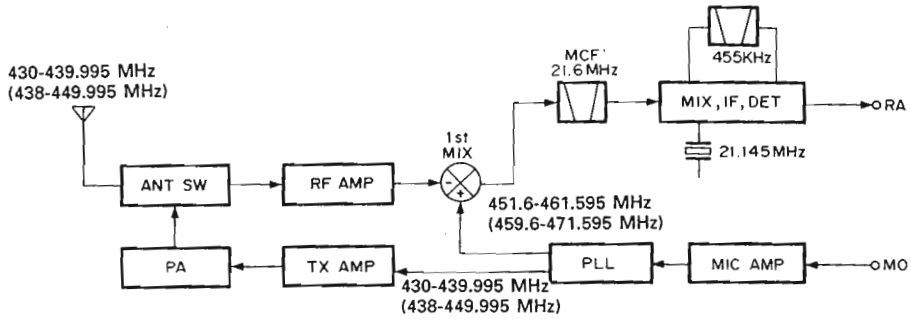
Table 16 PLL circuit pin functions

CIRCUIT DESCRIPTION

430 TX-RX Unit Frequency Configuration

The 430 MHz unit incorporates a digital variable-frequency oscillator (VFO) that can freely select a channel step of 5, 10, 12.5, 15, 20, or 25 kHz with a PLL synthesizer system. The frequency in the receive signal channel is mixed with a first local oscillation frequency of 451.6-461.595 MHz (459.6-471.595 MHz for K-models) to produce a first intermediate frequency of 21.6 MHz. The frequency is then mixed with a second local oscillation frequency of 21.145 MHz to produce a second intermediate frequency of 455 kHz. This is called a double-conversion system.

The signal in the transmission channel is directly oscillated and frequency-divided by a PLL circuit, amplified by a straight amplifier, then transmitted.



* The alphanumeric characters enclosed in parentheses are used for K-models.

Fig. 16 Frequency Configuration

430 TX-RX Unit Receive Signal Channel

- **Outline**

A 430 MHz band antenna input signal is passed through the antenna selection diode in the final stage and sent through a front-stage antenna matching coil to the high-frequency two-stage amplifier and helical block of a GaAs (gallium arsenide) FET and junction FET. The signal is then input to the first mixer. The first mixer input signal is mixed with the first local signal from the PLL circuit and converted to a first intermediate-frequency signal of 21.6 MHz. The unwanted near-by signal components are then eliminated by a two-stage MCF.

The first intermediate-frequency signal is amplified and input to FM IF HIC IC1 (KCD04). This signal is then mixed with a second local oscillation frequency of 21.145 kHz to produce a second intermediate frequency of 455 kHz. The unwanted near-by components of the intermediate-frequency signal are eliminated by an FM ceramic filter. The intermediate-frequency signal is input to IC1 again. The second intermediate-frequency signal is amplified and detected by IC1 to produce an audio signal.

- **Signal-strength meter**

The signal-strength meter output voltage of FM IF HIC IC1 (KCD04) is supplied to the control unit.

- **Shift-register circuit**

The ES, CK, and DT serial data from the control unit are sent to IC3 (BU4094BF) to perform the control operation outlined in the following table:

Pin No.	Name	Function	Pin No.	Name	Function
1	Strobe	Enable input	9	Q_S	
2	Data	Serial data input	10	Q'_S	
3	Clock	Clock input	11	Q8	
4	Q1	TX/RX selection. "L" when TX is set	12	Q7	
5	Q2	TX power selection. "L" when middle and low. "H" when high.	13	Q6	
6	Q3	TX power selection. "L" when high and low. "H" when middle.	14	Q5	
7	Q4		15	OE	8V
8	V_{SS}	GND	16	V_{DD}	8V

Table 17

CIRCUIT DESCRIPTION

430 TX-RX Unit Transmit Signal Channel

- **Outline**

In the transmission channel, the desired frequency is directly oscillated and directly frequency modulated by means of a varicap diode.

- **Modulator circuit**

The audio signal from the control unit is input to microphone amplifier HIC IC2 (KCA04). IC4 consists of a preemphasis circuit, amplifier, limiter, and splatter circuit that eliminate unwanted high-frequency components. The VCO signal is directly frequency modulated by a varicap diode in the frequency modulator circuit.

- **Younger-stage circuit**

The signal output from the VCO is input to drive circuit HIC IC6 (KCB14). The amplifier can obtain a stable drive output without adjustment because it has a wide band. An APC circuit controls the collector voltage in the younger final stage.

- **Power amplifier circuit**

A drive signal is input to power module IC7 and amplified to the specified level.

- **APC circuit**

The automatic transmission output control circuit (APC) detects and partially amplifies the power module output with a diode and controls the output control voltage. The control voltage is output in inverse proportion to the output, so the control voltage output is always constant. To protect the set against excessive temperature rise, the high-power unit has a thermal switch. The high-power unit is automatically set to a low power by the thermal switch when it exceeds the specified temperature.

430 TX-RX Unit PLL Synthesizer

The VCO and PLL circuit are housed in a solid shielding case as a hybrid integrated circuit. Comparison frequencies of 6.25 and 5 kHz are produced by dividing a 12.8 MHz reference oscillation frequency by 2048 and 2560 to correspond to 5, 10, 12.5, 15, 20, or 25 kHz channel steps.

For 430 MHz, the relationship between f_{VCO} (RX) and each frequency division ratio is given by

$f_{VCO} = (430 + 21.6) = \{(n \times 128) + A\} \times f_{OSC} \div R$

Where: f_{VCO} = VCO output frequency

n: Binary 10-bit programmable counter setting value

A: Binary 7-bit programmable counter setting value

f_{OSC} = Reference oscillation frequency of 12.8 MHz

R: Binary 14-bit programmable counter setting value

2560 (in 5, 10, 15,and 20 kHz steps)

2048 (in 12.5 and 25 kHz steps)

In 5, 10, 15, and 20 kHz steps, n is 705 and A is 80.

Therefore, $f_{VCO} = \{705 \times 128\} \times 12800 / 2560$

$= \{90240 + 80\} \times 5$

$= 451600$

$= 451.6$ MHz

See the 144 MHz band unit (X57-3580-00) for the function of each pin of IC10 in the PLL circuit.

- **8T (8 V during transmission) and unlock signal**

See the 144 TX/RX unit description on page 13. (The figure on the under indicates the 430 MHz unit.)

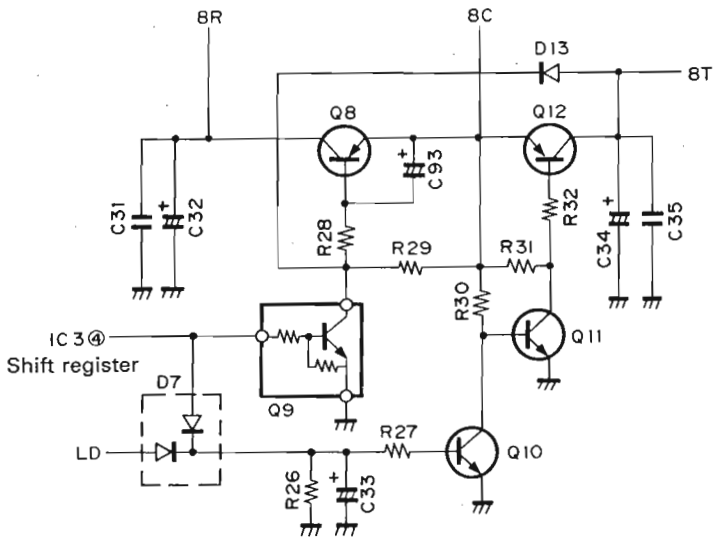


Fig. 17

CIRCUIT DESCRIPTION

TM-942A/UT-1200

1200 TX-RX Unit Frequency Configuration

The 1200 MHz unit incorporates a digital variable-frequency oscillator (VFO) that freely can select a channel step of 10, 12.5, 20,or 25 kHz with a PLL synthesizer system.

The frequency in the receive signal channel is mixed with a frequency of 1200.3 to 1240.20 MHz obtained when a first local oscillation frequency of 600.15 to 620.145 MHz is multiplied by 2 to produce a fist intermediate frequency of 59.7 MHz. This frequency is then mixed with a second local oscillation frequency of 59.245 MHz to produce a second intermediate frequency of 455 kHz. This is called a double-conversion system.

The signal in the transmission channel is oscillated and frequency-divided by a PLL circuit,then multiples the frequency of 630 to 649.995 MHz by two to produce a frequency of 1260 to 1299.99 MHz. This signal is amplified by a straight amplifier, then transmitted.

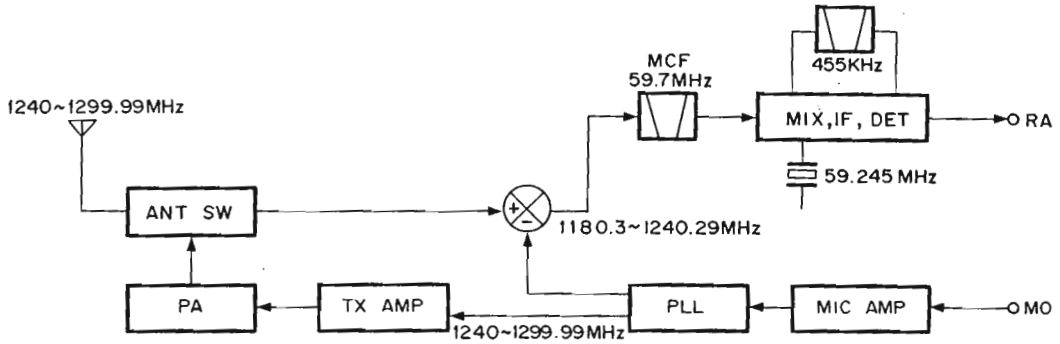


Fig. 18 Frequency Configuration

1200 TX-RX Unit Receive Signal Channel

- **Outline**

The received signal from an antenna is passed through a low-pass filter in the transmission final stage and sent through a transmission/reception selection diode switch to the receiving front end. The signal is then amplified to high frequencies by a microwave GaAs (gallium arsenide) FET and sent to a dielectric filter. The unwanted components of the signal are eliminated by a microwave transistor in another stage and the dielectric filter. The resultant signal is input to the first mixer. The front end block is matched by a microstrip line to ensure high sensitivity and high reliability. A GaAs FET is used in the first mixer to obtain a good two-signal characteristic. This signal is mixed with the first local signal from a PLL circuit by the first mixer and converted to a first intermediate frequency of 59.7 MHz. The unwanted near-by signal components are eliminated by a two-stage MCF. The resultant signal is produced as a first intermediate-frequency signal.

The first intermediate-frequency signal is amplified and input to FM IF HIC IC2 (KCD04). This signal is then mixed with a second local oscillation frequency of 59.245 kHz to produce a second intermediate frequency of 455 kHz. The intermediate-frequency signal is passed through a ceramic filter to obtain a sharp characteristic. The signal is then input to an HIC again, amplified, then demodulated and output from the HIC.

- **Signal-strength meter**

The signal-strength meter output voltage of FM IF HIC IC2 (KCD04) is supplied to the control unit.

- **Shift-register circuit**

The FS, CK, and DT serial data from the control unit are sent to IC5 (BU4094BF) to perform the control operation outlined in the following table:

CIRCUIT DESCRIPTION

Pin No.	Name	Function	Pin No.	Name	Function
1	Strobe	Enable input	9	Q_S	
2	Data	Serial data input	10	Q'_S	
3	Clock	Clock input	11	Q8	TX/RX selection. "L" when TX is set (Set low faster than Q1).
4	Q1	TX/RX selection. "L" when TX is set	12	Q7	ALT. "H" when on.
5	Q2	TX power selection. "L" when middle and low. "H" when high.	13	Q6	
6	Q3	TX power selection. "L" when high and low. "H" when middle.	14	Q5	
7	Q4		15	QE	8V
8	V_{ss}	GND	16	V_{DD}	8V

Table 18

1200 TX-RX Unit Transmit Signal Channel

- **Outline**

In the transmission channel, the desired frequency is oscillated by half and directly frequency modulated by means of a varicap diode.

- **Modulator circuit**

The audio signal from the control unit is input to microphone amplifier HIC IC4 (KCA04). IC4 consists of a preemphasis circuit, amplifier, limiter, and splatter circuit that eliminate unwanted high-frequency components. The VCO signal is directly frequency modulated by means of a varicap diode in the frequency modulator circuit.

- **Younger-stage circuit**

The signal output from the VCO is input to predrive circuit IC7 (KCB09). The amplifier can obtain a stable drive output without adjustment because it has a wide band.

- **Power amplifier circuit**

The signal amplified in the predrive stage is amplified again by drive circuit HIC IC8 (KCB10), then input to power module IC10 and amplified to the specified level.

- **APC circuit**

The automatic transmission output control circuit (APC) detects and partially amplifies the power module output with a diode and controls the output control voltage. The control voltage is output in inverse proportion to the output, so the control voltage output is always constant.

- **Antenna selection circuit**

Figure 19 shows the antenna selection circuit. The receiver circuit obtains a low insertion loss and isolation with a two-stage breaker circuit consisting of a λ/4 strip circuit.

The pin diode used as a switching device has a low junction capacitance. The high-frequency capacitance of the diode does not depend on the reverse bias voltage.

Figure 20 shows the equivalent circuit during transmission. A current flows through each diode using 8T. The impedance becomes very low. At that time, the receiver side uses a λ/4 strip circuit. Therefore, the impedance becomes very high when the receiver side is viewed from point (A). The voltage from a power module is transferred to the antenna.

Figure 21 shows the equivalent circuit during reception. The bias is switched off, so each diode is in a high-resistance state. The antenna and receiving circuit are connected by a strip line.

CIRCUIT DESCRIPTION

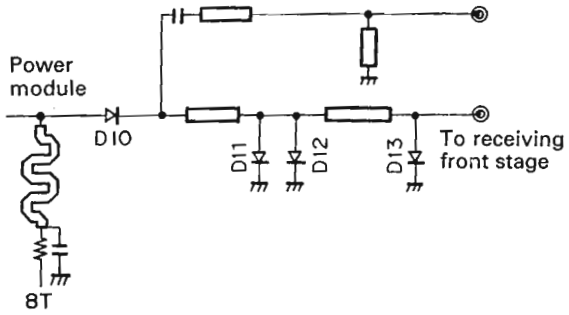


Fig. 19 Antenna Selection Circuit

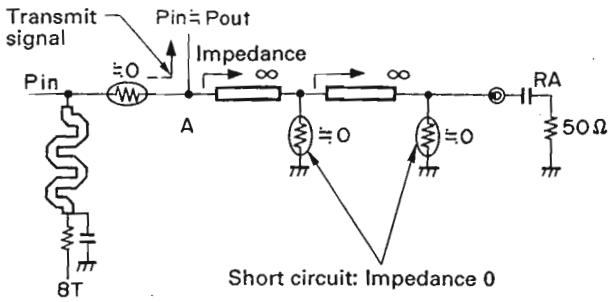


Fig. 20 Equivalent Circuit during Transmission

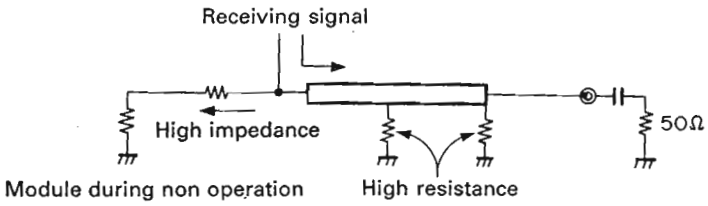


Fig. 21 Equivalent Circuit during Reception

1200 TX-RX Unit PLL Synthesizer

The VCO and PLL circuit are housed in .2 solid shielding case as a hybrid integrated circuit. This reduces the electrical and mechanical influence and ensures frequency stability.

The VCO and PLL circuit double the higher harmonics by oscillating and locking a 600 MHz frequency to produce a 1200 MHz band frequency. Comparison frequencies of 5 kHz and 6.25 kHz are produced by dividing a 12.8 MHz frequency of the TCXD by 2560 and 2048 to correspond to 10, 12.5, 20, and 25 kHz channel steps.

The relationship between f_{VCO} (RX) and each frequency division is given by

f_{VCO} (RX) = (f_{RX} – 59.7) / 2 = {(n × 128) + A} × f_{osc} ÷ R

Where: f_{VCO} (RX) = Previous output frequency that is multiplied by 2 during VCO reception

f_{RX} : Reception frequency

n : Binary 10-bit programmable counter setting value

A : Binary 7-bit programmable counter setting value

f_{osc}: Reference oscillation frequency of 12.8 MHz (TXCO)

R : Binary 14-bit programmable reference counter setting value

2048 (in 12.5 and 25 kHz steps)

2560 (in 10 and 20 kHz steps)

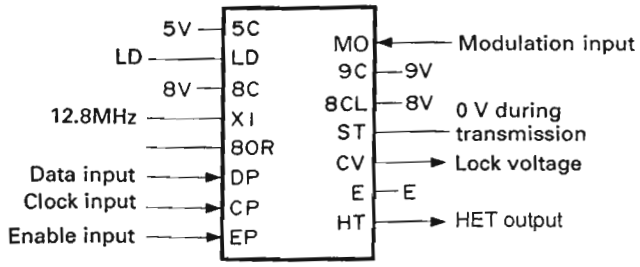
For 1260 MHz,

f_{VCO}(RX) = (1260 – 59.7)

= {(n × 180) + A} × 12800 ÷ 2560

= 600.15 MHz

In this case, n is 937 and A is 94.



The same as for the 144 MHz unit except 8 V shown in the figure above.

Fig. 22 PLL pin description

Pin name	Function	Pin name	Function
5C	5V	MO	Modulation signal input
LD	Lock signal (on during lock)	9C	9V
NC	Unused	8CL	8V (ripple filter)
XI	12.8 MHz crystal oscillation	ST	0 V during transmission
80R		CV	Lock voltage
DP	Data input	E	GND
CP	Clock input	HT	HET output
EP	Enable input		

Table 19

CIRCUIT DESCRIPTION

- **Unlock circuit**

When a PLL circuit is unlocked during transmission, the LD pin of a IC11 set low and Q12 is set off. Q11 is then set on. The 8T line is not activated when 8T switching control circuit Q13 is set off.

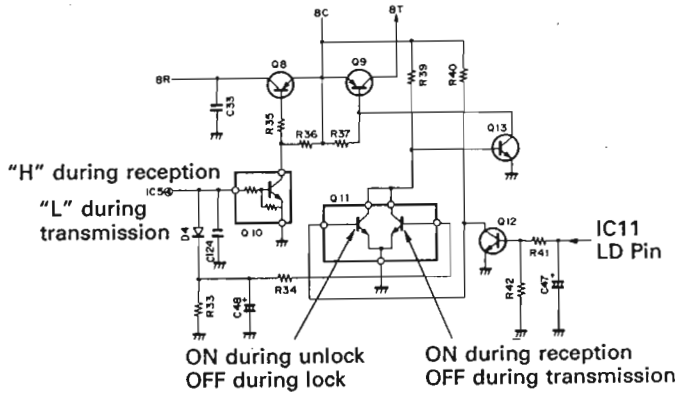


Fig. 23 Unlock Circuit

- **Predrive circuit HIC (KCB09)**

The VCO output is amplified by Q22, then input to pre-drive circuit HIC IC7. An average 22 to 23 dBm output is obtained by inputting 0 dBm through three-stage (2SC4093 and 2SC3357 x 2) amplification. An alumina board and hybrid integrated circuit are used to ensure stable circuit operation.

- **Drive circuit HIC (KCB10)**

The VCO output is amplified by KCB09, then input to drive circuit HIC. An average 29 dBm output is obtained by inputting 20 dBm through one-stage (2SC3814) amplification. An integrated radiation plate and alumina board are used to attain a stable output against heating.

- **ALT (Automatic Frequency Locked Tuning) Circuit**

The block diagram of the ALT unit is shown in **Fig. 24**

The ALT system uses a portion of the second local oscillator signal, mixer, and the FM IF HIC: KCD04 module to form a feed-back circuit that is used to provide analog automatic frequency control.

When the first IF (59.7 MHz) changes due to a shift in the transmitter frequency a corresponding shift will occur in the second intermediate frequency. A portion of this second IF signal is detected. This correction voltage is amplified (NJM4558M) and is used to control D1 and D2 via analog switch MN4066BS. TP1 can be used to check the value of this control voltage. D1 and D2 are in series with the 59.245 MHz oscillator circuit and provide voltage control of this oscillator (VCXO, Voltage controlled oscillator). Therefore, fluctuations of the second IF cause a corresponding change in the second local oscillator circuit, which keeps the frequency of the second IF within the bandwidth of the IF filter. This system maintains close agreement between the transmit and receive frequency bandwidths. (In practice, the receiver frequency and transmit frequency are automatically maintained in close agreement.) The center voltage of the vari-cap diode is set by a voltage divider circuit. Stability of this voltage is maintained by a voltage follower circuit. When the ALT circuit is off, the control voltage applied to the vari-cap diode is switched to this fixed voltage divider circuit in order to set the second local oscillator frequency.

The control voltage for the vari-cap diode is subject to one additional voltage divider stage. During receive this DC signal is applied from the RM line to the microprocessor terminal PTH02 which turns on the tuning indicator light. Switching is performed by the 8R line.

The relationship between the input voltage on the PTH02 terminal and the tuning indicator, and the relationship between the RM voltage and the deviation during receive is shown in **Table 20** and **Fig. 25**

CIRCUIT DESCRIPTION

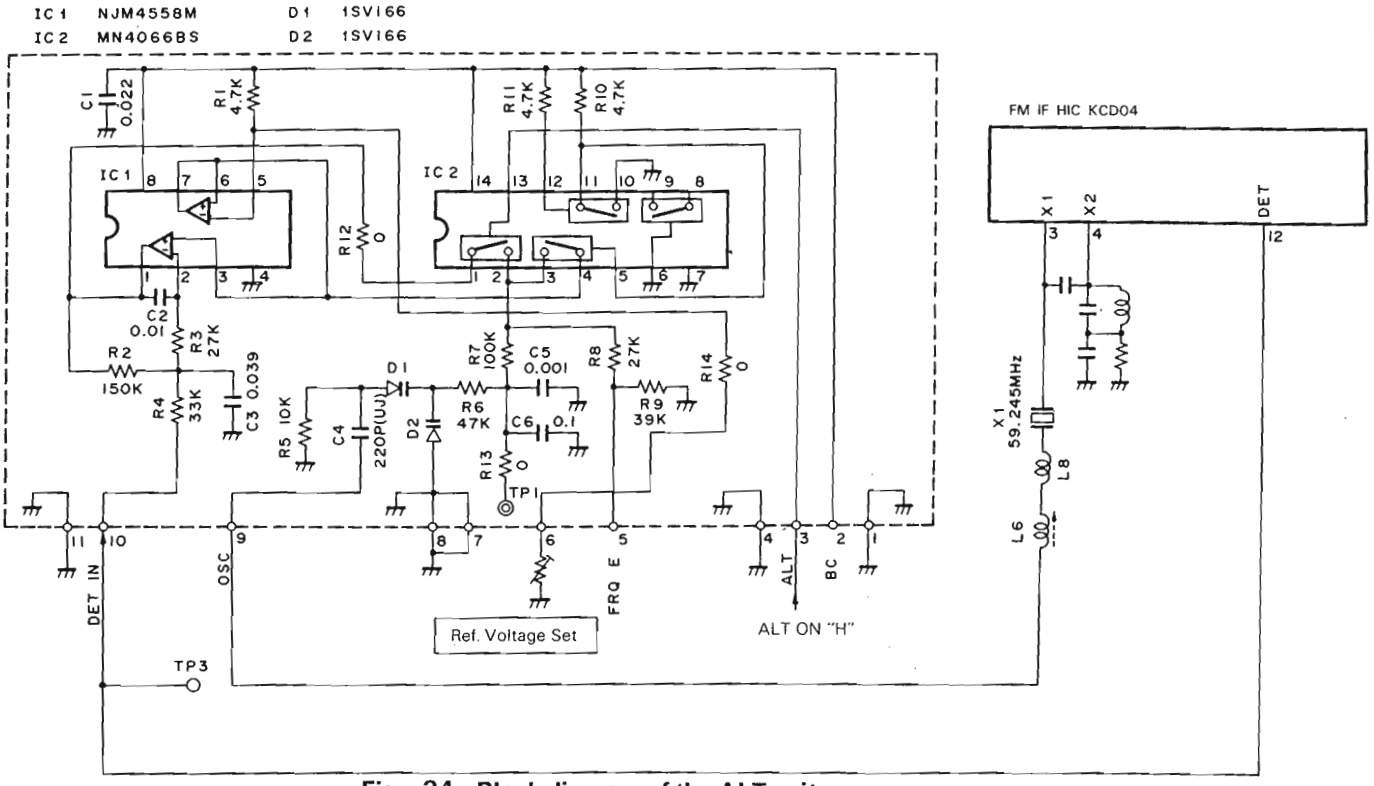


Fig. 24 Block diagram of the ALT unit

PTH02 input voltage	ALT indicator
0~1.48 V	Only ◁ turns ON
1.48~2.79 V	Both ◁ and ▷ turn OFF
2.79~5.0 V	Only ▷ turns ON

Table 20 Relationship between PTH02 input voltage and the T indicator

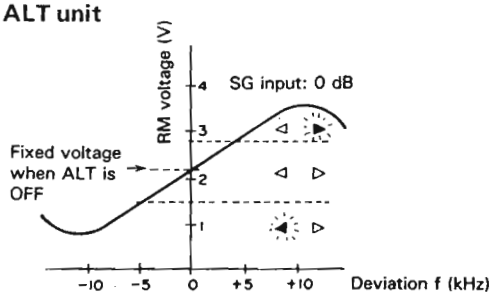


Fig. 25 Relationship between the RM voltage and deviation during receive

DIGITAL CONTROL UNIT

• OUTLINE

The digital control unit consists of the panel unit which comprises the keys, rotary encoder circuit and display circuit, as well as the control unit which comprises the reset backup circuit, the DTMF circuit, the microphone key input circuit, the dimmer circuit, etc.

• DATA COMMUNICATION CIRCUIT OF THE PANEL CONTROL UNIT

Figure 26 shows the data communication circuit of the panel control unit. So is the serial data output, SI is the serial data input, and an inverter is located between them to protect the ports of the microprocessor.

The data communication system is asynchronous, and a communication rate of 31250bps is realized.

Since the connection is checked once every 0.5 second by the microprocessor of the control unit side, the power turns OFF when the panel unit is removed.

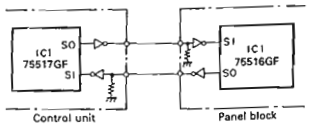


Fig. 26

CLOCK IC

INITIALIZATION

• SYSTEM RESET

The POWER ON CLEAR function works automatically and all logics are initialized in this IC (S-3520CF) when the power is turned ON. The system is reset because the POWER ON CLEAR bit (D2 of the CNT2 register) is stuck at "1".

• SYSTEM RESET

All logics are initialized when the SYSCR bit is set to "1". When cancelling the reset, SCK falls down after the build-up of CS, as shown in Figure 27.

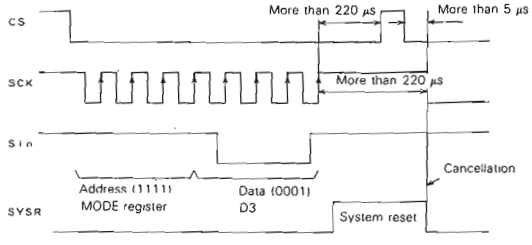


Fig. 27 Reset cancellation timing

CIRCUIT DESCRIPTION

• INITIAL SETTING

MODE SETTING REGISTER

The clock mode is selected by entering the address 1111 and data 0000 (Ordinary-mode/Clock-mode selection) from Sin. (Refer to DATA WRITE for the entry of data).

CONTROL REGISTER 1

Address 1101 and data 1001 (reference signal output waveform 1 Hz, 24-hour display system) is entered from Sin.

DATA CONTROL

• DATA READ

The read mode is set by sticking CS at "L" and WR at "H". The serial address is entered from Sin, at the leading edge of the upper 4 bits of the SCK clock. (The other 4 bits have nothing to do with this operation). When WR is fetched at the 8th leading edge of the SCK clock, the entered address and its data are outputted from Sout, synchronized with the leading edge of the SCK clock. (Figures 28, 29).

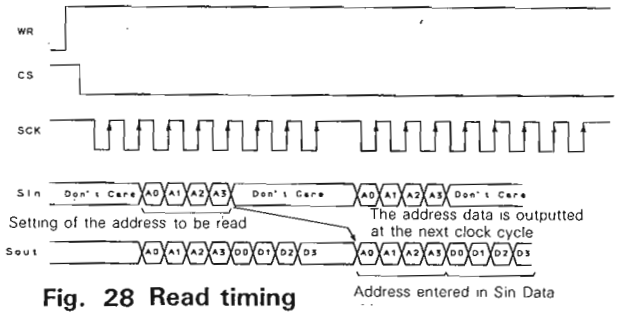


Fig. 28 Read timing

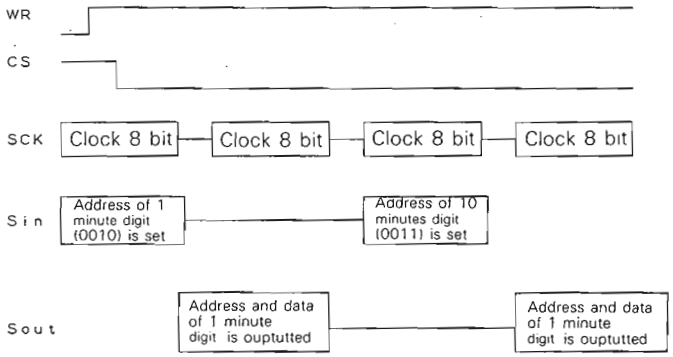


Fig. 29

• DATA WRITE

The WRITE mode is set by sticking CS to "L" and WR to "L". When the serial address and the data to be written (it is not necessary to write it in the counter) are entered from Sin, they are fetched at the leading edge of the SCK clock. When WR is fetched with the 8th leading edge fo the CSK clock, the following data is written in the entered address.

Counter: Increment of the data
Register: 4-bit data entered form Sin
Figure 30, 31 shows the writing timing.

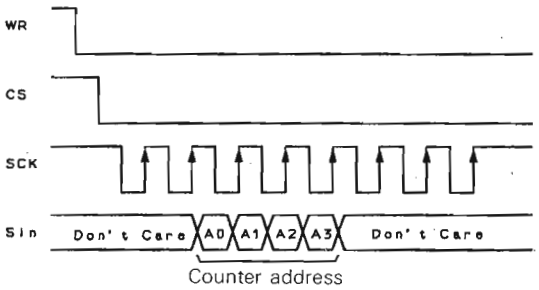


Fig. 30 Counter write timing

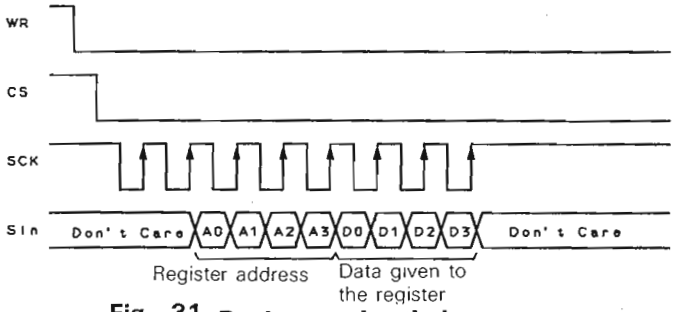


Fig. 31 Register write timing

• EXAMPLE OF DATA WRITING

Example of counter writing.

Figure 32 shows the example which consists of writing the "minute" column.

Example of register writing.

Figure 33 shows the example which consists of writing in the control register 1.

(Refer to the reset backup circuit for the backup).

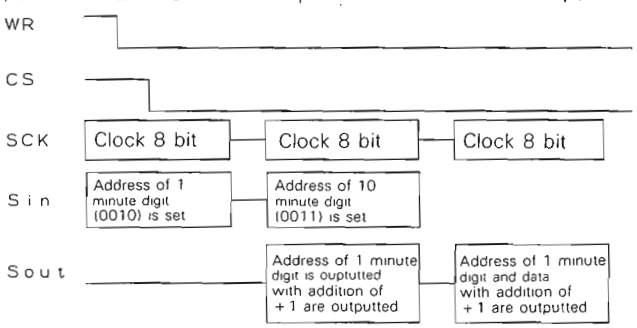


Fig. 32

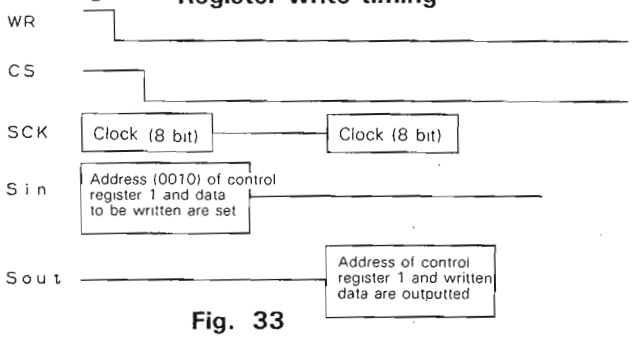


Fig. 33

CIRCUIT DESCRIPTION

PANEL UNIT

• KEY ROTARY ENCODER INPUT CIRCUIT

Each key of the panel unit is inputted in one port. Moreover, the rotary encoder is directly inputted in the microprocessor.

• DISPLAY CIRCUIT

The display circuit consists of two LCD dirvers located at the panel unit and their peripheral circuits (Figure 34), and all processings are carried out by the microcomputer located at the panel side.

The LCD features dynamic lighting up with 1/2 duty, and the lighting up contents are sent from the CPU (IC1: HD404719A26H) to the LCD by serial data transfer.

The LCD display consists of 158 segments.

• DESCRIPTION OF THE OPERATION

Normally, the CLOCK line is stuck at "L" and the DATA line is stuck at "H".

Since the shift register consists of 160 + 160 bits = 320 bits in series, it must be given 320 bit data every time.

For the ENABLE signal to be outputted, the DATA line is switched H/L 4 times at the point (A) (B), with the CLOCK line stuck at "H" after transmitting 320 bits for MSM5265,

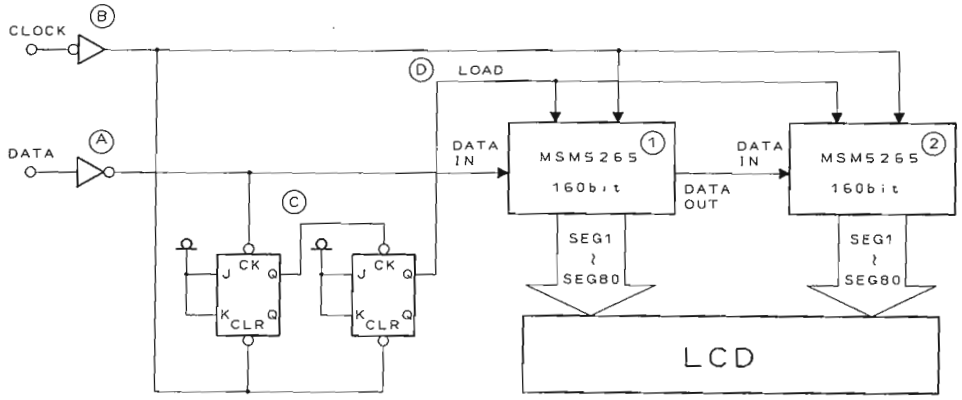


Fig. 34 Display Circuit

• DIMMER CIRCUIT

The dimmer circuit changes the brightness of the lamps in 6 steps

Figure 35 shows the dimmer circuit, which is built into the IC114 (HIC).

A voltage changeable in 6 steps is outputted from the LB port through the combination of the various LB ports (Q1 to Q3) of the shift register. (Refer to the Shift Register Port Table for the logic).

The display does not light up when the power is turned OFF, because the LB line is switched by means of the LB switch: Q2.

• Control band LED lighting circuit

The LED brightness is changed by switching the current to one of two ports for each LED. It is changed in two steps corresponding to lamp dimmers d1, d2, and d3, d4.

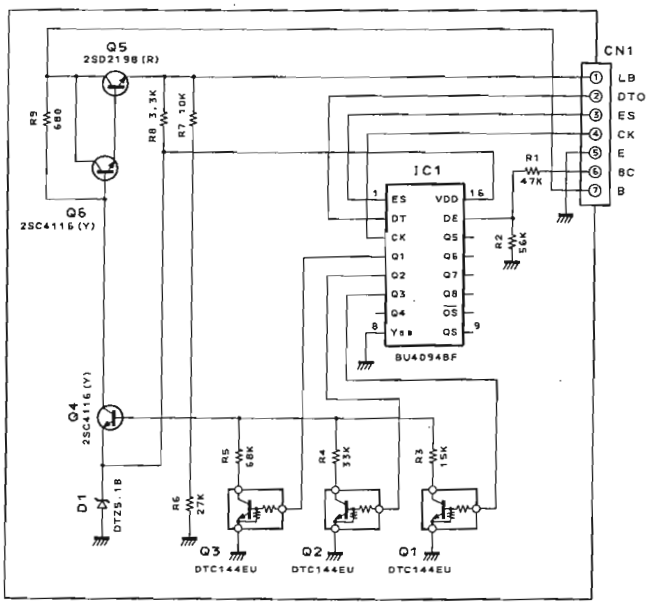


Fig. 35 Dimmer Circuit

CIRCUIT DESCRIPTION

• Squelch volume input

The squelch volume for each band works by converting the voltage output by dividing 5 V applied to the variable resistor at the analog port of the microprocessor, and so reads the rotation angle. If the rotation angle changes, a command corresponding to the value is sent to the control unit.

CONTROL UNIT

• RESET BACKUP CIRCUIT

The "L" level pulse with duration of approximately 20ms is outputted by the RESET IC (IC12) and the RESET SW (Q5) when the power is turned ON. The CPU is reset by means of this pulse.

When the power is turned OFF, the voltage drop of the 13.8V line is detected, Q6 of the backup circuit turns OFF, Q9 turns ON, and the IRQ terminal is stuck at the "L" level. As a result, the CPU gets in the backup operation. At that time, the voltage VDD is supplied by BAI vis R24/D1. Moreover, the backup circuit is also connected to the clock IC: IC6 (S-3520CF) , and it gets in the access inhibit (backup) state when the "L" level is entered. Refer to the Port List for IC6.

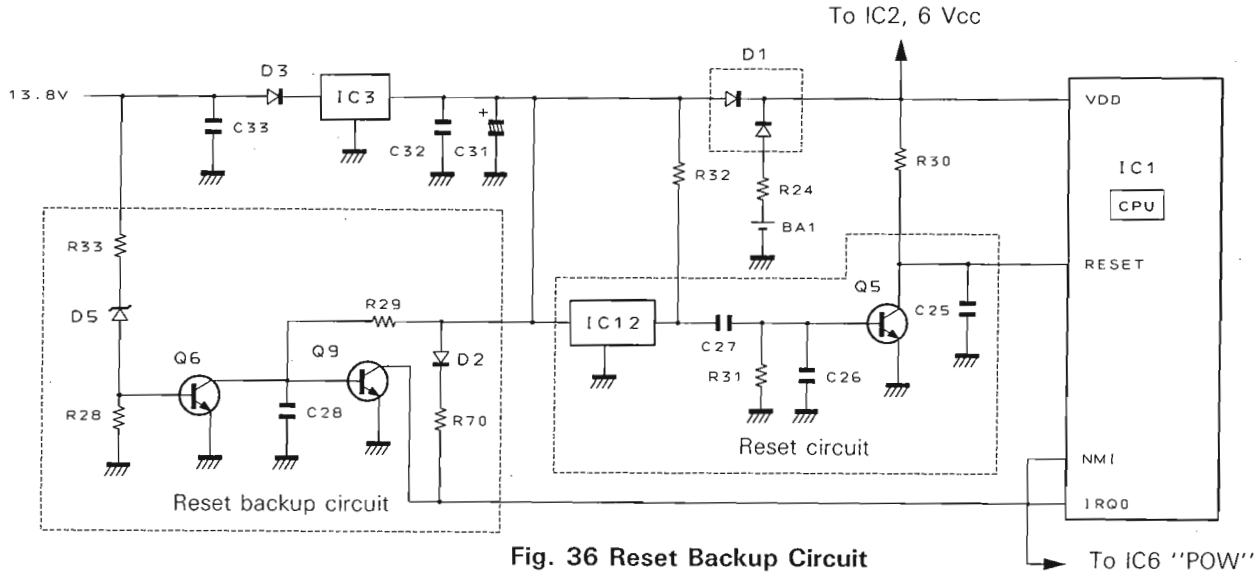


Fig. 36 Reset Backup Circuit

• MICROPHONE/KEY INPUT CIRCUIT

The UP/DOWN keys and the function keys of the microphone are connected to the analog inputs of the microprocessor, and the various functions are operated by the voltage applied when the key is ON. (Figure 37)

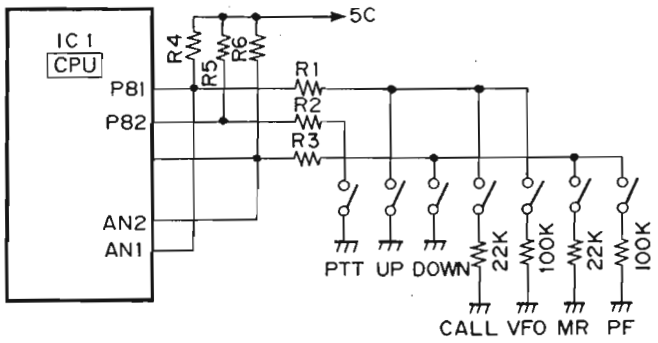


Fig. 37 Microphone key input circuit

• SHIFT REGISTER

Processing of the dimmer, squelch and level functions is carried out by passing serial data from the microprocessor through the shift registers located in IC113 and IC114 (BU4094BF).

The dimmer and the squelch levels are set by 24-bit control, by using 3 shift registers.

The first 8 bits of the 24 bits are the dimmer level setting data (shift register C), and the remaining 16 bits are the squelch level setting data (shift registers A, B). (Figure 38)

CIRCUIT DESCRIPTION

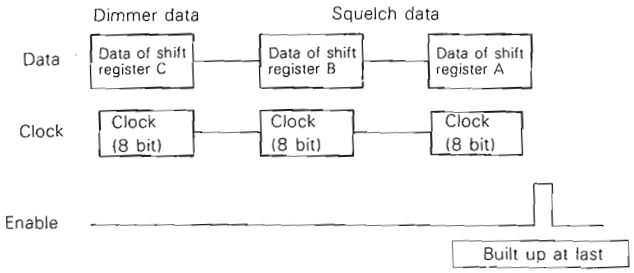


Fig. 38

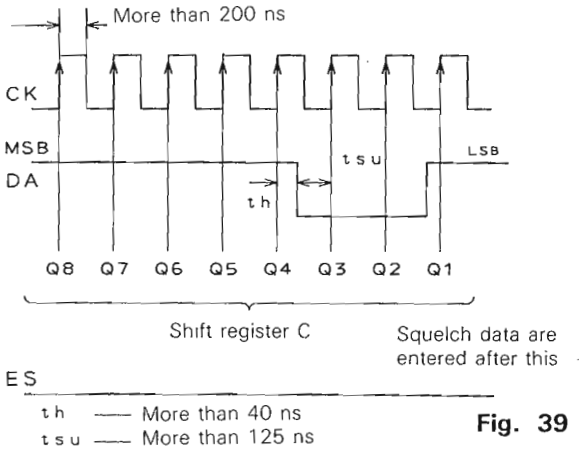


Fig. 39

The dimmer level setting is carried out by using 3 bits out of the 8 bits of the shift register. The remaining 5 bits (Q4 to Q8) are open ports, and they are stuck at "H" during data transmission. (Figure 39)

The squelch level is set by using the 16-bit data that follow the 8-bit data used for setting the dimmer level. (Figure 40)

Refer to the SHIFT REGISTER PORT SPECIFICATION LIST for the port specifications of each shift register.

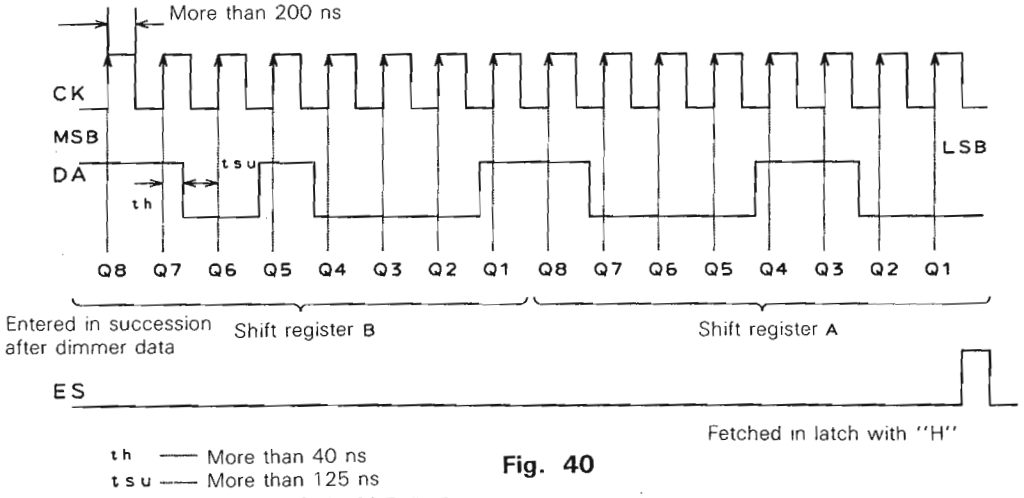


Fig. 40

SHIFT REGISTER PORT SPECIFICATION LIST (VOL, SQ HIC) CONTROL UNIT (X53-346X-XX)

SHIFT REGISTER A 4094: BUILT INTO IC113

S. Reg Port	Pin No.	Port Data Name	SAVE	Backup	Function	Circuit Terminal name
Q1	4	PD__RDMUT			RD mute 0: ON 1: OFF	RD MUTE
Q2	5	PD__SQA0			BAND A squelch level adjustment (bit 0) 0: There is resistance 1: No resistance	
Q3	6	PD__SQA1			BAND A squelch level adjustment (bit 1) 0: There is resistance 1: No resistance	
Q4	7	PD__SQA2			BAND A squelch level adjustment (bit 2) 0: There is resistance 1: No resistance	
Q5	14	PD__SQA3			BAND A squelch level adjustment (bit, 3) 0: There is resistance 1: No resistance	
Q6	13	PD__SQA4			BAND A squelch level adjustment (bit 4) 0: There is resistance 1: No resistance	
Q7	12	PD__SQB0			BAND B squelch level adjustment (bit 0) 0: There is resistance 1: No resistance	
Q8	11	PD__SQB1			BAND B squelch level adjustment (bit 1) 0: There is resistance 1: No resistance	

CIRCUIT DESCRIPTION

Shfit registor B 4094

S. Reg Port	Pin No.	Port Data Name	SAVE	Backup	Function	Circuit Terminal name
Q1	4	PD__SQB2			Band B squelch level adjustment (bit 2) 0: There is resistance 1: No resistance	
Q2	5	PD__SQB3			BAND B squelch level adjustment (bit 3) 0: There is resistance 1: No resistance	
Q3	6	PD__SQB4			BAND B squelch level adjustment (bit 4) 0: There is resistance 1: No resistance	
Q4	7	PD__SQC0			BAND C squelch level adjustment (bit 0) 0: There is resistance 1: No resistance	
Q5	14	PD__SQC1			BAND C squelch level adjustment (bit 1) 0: There is resistance 1: No resistance	
Q6	13	PD__SQC2			BAND C squelch level adjustment (bit 2) 0: There is resistance 1: No resistance	
Q7	12	PD__SQC3			BAND C squelch level adjustment (bit 3) 0: There is resistance 1: No resistance	
Q8	11	PD__SQC4			BAND C squelch level adjustment (bit 4) 0: There is resistance 1: No resistance	

All bits are stuck at "H" (H'IF) when MONI ON.
Data coming from the panel are inverted when they enter the shift register.

CONTROL UNIT (X53-346X-XX)
SHIFT REGISTER C 4094: BUILT INTO IC114

S. Reg Port	Pin No.	Port Data Name	SAVE	Backup	Function	Circuit Terminal name
Q1	4	PD__			For dimmer level adjustment (Bit 0) Refer to the table below for the logic.	
Q2	5	PD__			For dimmer level adjustment (Bit 1) Refer to the table below for the logic.	
Q3	6	PD__			For dimmer level adjustment (Bit 2) Refer to the table below for the logic.	
Q4	7	PD__			Open port, the bit is stuck at "1"	
Q5	14	PD__			↑	
Q6	13	PD__			↑	
Q7	12	PD__			↑	
Q8	11	PD__			↑	

Data coming from the panel are inverted when they enter the shift register.

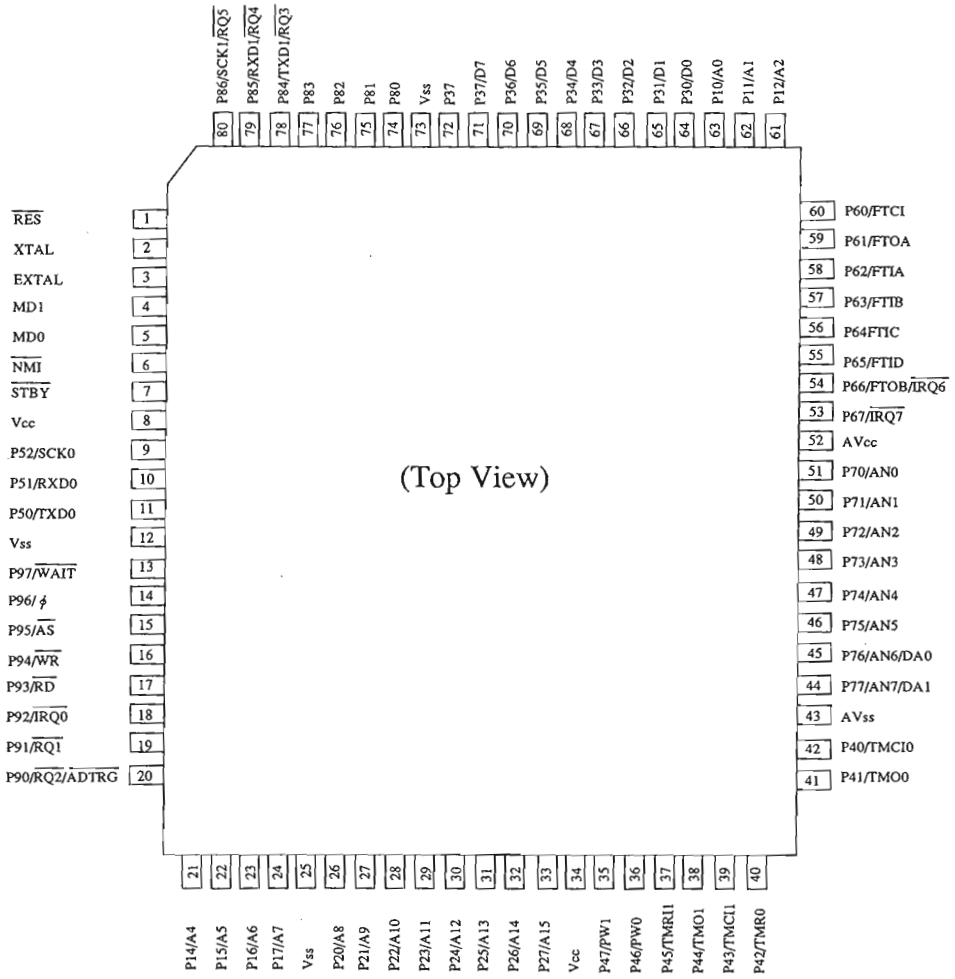
Port logic versus dimmer level correspondence lit

Dimmer level	Q3 (bit 2)	Q2 (bit 1)	Q1 (bit 0)
d1	0	1	0
d2	0	1	1
d3	1	0	0
d4	1	0	1
d5	1	1	0
d6	1	1	1

CIRCUIT DESCRIPTION

I/O PORT SPECIFICATION LIST

CONTROL UNIT (X53-346X-XX): IC1 (HD6433388A04F)



HD6433388A04F I/O PORT LIST: IC1

μCOM Port	Port Name	I/O	Pull up	Back up	Control	Circuit Terminal name
RES	P__RES	I			Reset terminal 0: Reset state 1: Ordinary state	
MD1	P__MD1	I			Operation mode (Mode 2) setting. Set to 1	
MD0	P__MD0	I			Operation mode (Mode 2) setting. Set to 0	
STBY		I			Set to 1	
P10 A0	P__A0	O		I	External RAM, I/O Expander Address	
P11 A1	P__A1	O		I	↑	
P12 A2	P__A2	O		I	↑	

CIRCUIT DESCRIPTION

HD6433388A04F I/O PORT LIST

μCOM Port	Port Name	I/O	Pull up	Back up	Contents	Circuit Terminal name
P13 A3	P__A3	O		I	External RAM Address	
P14 A4	P__A4	O		I	↑	
P15 A5	P__A5	O		I	↑	
P16 A6	P__A6	O		I	↑	
P17 A7	P__A7	O		I	↑	
P20 A8	P__A8	O		I	↑	
P21 A9	P__A9	O		I	↑	
P22 A10	P__A10	O		I	↑	
P23 A11	P__A11	O		I	↑	
P24 A12	P__A12	O		I	↑	
P25 A13	P__RAMCE2	O		I	External RAM CE2	CE2
P26 A14	P__RAMCE11	O		I	External RAM CE1 Input composing AND with P__RAMCE12	CE1
P27 A15	P__RAMCE12	O		I	External RAM CE1 Input composing AND with P__RAMCE11	↑
P30 D0	P__DAT0	I/O		I	External RAM, I/O Expander data	
P31 D1	P__DAT1	I/O		I	↑	
P32 D2	P__DAT2	I/O		I	↑	
P33 D3	P__DAT3	I/O		I	↑	

CIRCUIT DESCRIPTION

HD6433388A04F I/O PORT LIST

μCOM Port	Port Name	I/O	Pull up	Back up	Content	Circuit Terminal name
P34 D4	P_DAT4	I/O		I	External RAM, I/O Expander data	
P35 D5	P_DAT5	I/O		I	↑	
P36 D6	P_DAT6	I/O		I	↑	
P37 D7	P_DAT7	I/O		I	↑	
P40 TMC10	P_CKCS	O		I	Clock chip select S3520CF CS — 0: Selected state 1: High impedance	
P41 TMO0	P_CKSOUT	I		I	Clock data input S3520CF SOUT	
P42 TMRI0	P_CKWR	O		I	Clock write select S3520CF WR — 0: Write 1: Read	
P43 TMCI1	P_CKSIN	O		I	Clock data output/CTCSS Unit Data S3520CF SIN	
P44 TMO1	P_BEEP	O		I	"Beep" sound output terminal (Effect sound) — Stuck at the "L" level when there is no output of the "Beep" sound.	BZ
P45 TMRI0	P_PSW	O		I	Power switch. — 0: Power ON 1: Power OFF	PSW
P46 PW0	P_TONE	O		I	Sub-tone	
P47 PW1	P_CKSCK	O		I	Clock synchronism signal output (S3520Cf SCK)/Serial→Parallel conversion (HD74HC165F)/CTCSS Unit Clock	
P50 TXD0	P_SO	O	●		Panel microprocessor SI	
P51 RXD0	P_SI	I	●		Panel microprocessor SO	
P52 SCK0	P_Q165	I			Parallel→Serial conversion (HD74HC165F) input Destination, repeater function provided/not-provided, FAN SW, etc.	
P60 FTC1	P_DTDA0	I/O		I	DTMF Data (D4/Q1)	
P61 FT0A	P_DTDA1	I/O		I	DTMF Data (D3/Q2)	

CIRCUIT DESCRIPTION

HD6433388A04F I/O PORT LIST

μCOM Port	Port Name	I/O	Pull up	Back up	Content	Circuit Terminal name
P62 FTIA	P__DTDA2	I/O		I	DTMF Data (D2/Q3)	
P63 FTIB	P__DTDA3	I/O		I	DTMF Data (D1/Q4)	
P64 FTIC	P__STD	I		I	DTMF detection (LC7385 StD) 0: No signal 1: Signal detected	DV
P65 FTID	P__DTSEL	O		I	DTSS unit switching 0: Detection output 1: MIC	DTSEL
P66 FT0B IRQ6	P__DTCE	O		I	DTMF tone generator TC35219 TOE 0: No output a: Tone output	CE
P67 IRQ7	P__DTOE	O		I	DTMF receiver LC7385 TOE 0: High impedance 1: Enable	EN
P70 AN0	P__DOWN	O	•	I	Mic. DOWN (Port shared with RXD1) MR, PF	
P71 AN1	P__UP	I	•	I	Mic. UP (Port shared with SCK1) CALL, VFO	
P72 AN2	P__ALTA	I		I	BAND Unit A ALT input	
P73 AN3	P__ALTB	I		I	BAND Unit B ALT input	
P74 AN4	P__ALTC	I		I	BAND Unit C ALT input	
P75 AN5	P__SMA	I		I	BAND Unit A S meter input	
P76 AN6	P__SMB	I		I	BAND Unit B S meter input	
P77 AN7	P__SMC	I		I	BAND Unit C S meter input	

CIRCUIT DESCRIPTION

HD6433388A04F I/O PORT LIST

μCOM Port	Port Name	I/O	Pull up	Back up	Content	Circuit Terminal name
P80	P__ET	O I	●	I	CTCSS Unit Enable conenection check 0: CONNECT 1: NO CONNECT	ET
P81	P__CTCSS	I		I	CTCSS DETECT 0. Tone coincidence 1: No tone coincidence	SDO
P82	P__MMUTE	O		I	Mic MUTE 0: MUTE OFF 0: MUTE ON	
P83	P__KBRD	I	▲	I	CONTROLLER CHECK 1 NEW KENWOOD BUS (RD)	KBRD
P84 TXD1 IRQ3	P__KBSO (P__PTT)	I/O	●	I	NEW KENWOOD BUS (SO) 0 Mic. PTT 1	KBSO
P85 RXD1 IRQ4	P__KBSI	I	●	I	NEW KENWOOD BUS (SI) 1 Shared with Mic. DOWN terminal (AN0)	KBSI
P86 SCK1 IRQ5	P__KBCK	I/O	●	I	NEW KENWOOD BUS (Clock) 1 Shared with Mic. UP terminal (AN1)	KBCK
P90 ADTRG IRQ2	P__RPTON	O		I	Operation of REPEATER function 0: ON 1: OFF	
P91 IRQ1	P__TPOUT	I		I	Clock reference signal input S-3520 TPout	
P92 IRQ0	P__VF	I		I	Power check 0: During backup 1: During operation	
P93 RD	P__RD	O		I	External RAM, I/O Expander read control signal 0: External read 1: Inhibit	
P94 WR	P__WR	O		I	Externla RAM, I/O Expander write control signal 0: External read 1: Inhibit	

△: Pull-up only when checked by software. (Care must be taken, because P__ET is stuck at "H" during check).
○: Pull-up only when stuck at "H", during input with software.
●: Pull-up with hardware.
▲: Pull-down with hardware.

CIRCUIT DESCRIPTION

I/O EXPANDER PORT SPECIFICATION LIST

CONTROL UNIT (X53-346X-XX)

CXD1095Q I/O PORT LIST IC101

Port	I/O	Backup	Content	Circuit terminal name
PA0	O		Operation unit switching of CTCSS *1	CTC1
PA1			Operation unit switching of CTCSS *1	CTC2
PA2			Detection output connection unit switching *3	RD1
PA3			Detection output connection unit switching *3	RD2
PA4	O		Operation unit switching of DTSS *2	DTS1
PA5			Operation unit switching of DTSS *2	DTS2
PA6			FAN ON/OFF 0: OFF 1: ON	FANSW
PA7			Power switch other than 5C 0: OFF 1: ON	PWS2
PB0	O		Volume, squelch HIC Data	VOLSQDA
PB1			Volume, squelch HIC Clock	VOLSQCK
PB2			Squelch Enable 0: No change 1: Data fetched in latch	SQES
PB3			Electronic volume 2 Enable. Data latch at (1→0)	VOLCSA
PB4	O		Electronic volume 1 Enable. Data latch at leading edge (1→0)	VOLCSB
PB5			BEEP MUTE BAND A 0: MUTE OFF 1: MUTE ON	MUTEA
PB6			BEEP MUTE BAND C 0: MUTE OFF 1: MUTE ON	MUTEC
PB7			BEEP MUTE BAND B 0: MUTE OFF 1: MUTE ON	MUTEB
PC0	I		BAND Unit A busy input 0: BUSY 1: CLOSE	SCA
PC1			BNAD Unit B Busy input 0: BUSY 1: CLOSE	SCB
PC2			BNAD Unit C Busy input 0: BUSY 1: CLOSE	SCC
PC4	I/O		BAND Unit A shift Register Enable	ESA
PC5			BAND Unit A PLL/Shift Register Data *1	DTA
PC6			BAND Unit A PLL/Shift Register Clock *1	CKA
PC7			BAND Unit A PLL Enable *1	EPA
PD0	I/O		BAND Unit B Shift Register Enable	ESB
PD1			BAND Unit B PLL/Shift Register Data *2	DTB
PD2			BAND Unit B PLL/Shift Register Clock *2	CKB
PD3			BAND Unit B PLL Enable *2	EPB
PD4	I/O		BAND Unit C Shift Register Enable	ESC
PD5			BAND Unit C PLL/Shift Register Data *3	DTC
PD6			BAND Unit C PLL/Shift Register Clock *3	CKC
PD7			BAND Unit C PLL Enable *3	EPC

CIRCUIT DESCRIPTION

CXD1095Q I/O PORT LIST

Port	I/O	Backup	Content	Circuit terminal name
PE0	O		Shift Register (HD74HC165F) S/L terminal 0: Latch asynchronous with clock 1: Latch at loading edge of clock	LOAD165
PE1	O		AF MUTE BAND A 0: MUTE OFF 1: MUTE ON	
PE2	O		AF MUTE BAND B 0: MUTE OFF 1: MUTE ON	
PE3	O		AF MUTE BAND C 0: MUTE OFF 1: MUTE ON	

*1, *2, *3 Types of band units

BAND Unit	EP X	CK X	DT X	Unit No.	Number after conversion
No unit	0	0	0	0	0
28 MHz BAND	0	0	1	1	1
50 MHz BAND	0	1	1	3	2
144 MHz BAND	1	1	0	6	3
220 MHz BAND	0	1	0	2	4
430 MHz BAND	1	0	1	5	5
1200 MHz BAND	1	0	0	4	6

NOTE: X is A, B or C

The number after conversion is used on the program

*1, *2, *3

CTC2	CTC1	CTCSS opcration unit
DTS2	DTS1	DTSS operation unit
RD2	RD1	Detected output connection unit
0	0	A
0	1	B
1	X	C

CIRCUIT DESCRIPTION

TERMINAL LIST OF CLOCK IC (S-3520CF)
CONTROL UNIT (X53-346X-XX)

SERIAL TIME CLOCK (S-3520CF): IC6

Terminal No.	Name	Function	H8/337 connection terminal name
4	SCK	Synchronous signal input terminal of serial I/O 8 clocks/cycle	P47
5	Sin	Serial address/data input terminal Entry of address of counter or address/data of register/RAM.	P43
9	Sout	Serial address/data output terminal.	P41
6	WR	Write selection terminal. WR = "L": Write WR = "H": Read	P42
11	CS	Chip select terminal CS = "L": Selected state CS = "H": Sout gets at high impedance state	P40
10	PDW	System power supply leading edge check signal. Connected to power down detection circuit Stuck at "H" when PDW is not used Access disable irrespective of CS when fixed PSW = "L". (Sout, TPout get at high impedance state).	—
8	TPout	Reference signal output terminal, 1 Hz/1024Hz switching output.	P91

Control Unit (X53-346X-XX): IC6 (S-3520CF)
ADDRESS CORRESPONDENCE LIST

Address (A3 to A0)	Clock mode (MODE 0)
0000	1-second column counter
0001	10-second column counter
0010	1-minute column counter
0011	10-minute column counter
0100	1-hour column counter
0101	10-hour column counter
0110	Day (of the week) counter
0111	1-day column counter
1000	10-day column counter
1001	1-month column counter
1010	10-month column counter
1011	1-year column counter
1100	10-year column counter
1101	Control register 1
1110	Control register 2
1111	Mode setting register

The contents of the counter and the register can be read and rectified by handling the 4-bit address and data as a set. The addresses are allocated as shwon in the table below.

REGISTER CONTROL

• MODE SETTING REGISTER

Switches the clock mode and the SRAM mode, and resets the system.

MODE SETTING REGISTER (MODE, 1111)

D3	D2	D1	D0
SYSR	TEST	MS1	MS0

0 fixed Clock mode selected "00" entered

SYSR is used to clear the counter and the register. The system is reset when it is stuck at "1", and gets at the ordinary mode when it is stuck at "0".

MS0 and MS1 are used to switch the mode. Since the clock mode is used this time, "0""0" is entered in these registers

CONTROL REGISTER 1 (CNT1, 1101)

D3	D2	D1	D0
TPS	30ADJ	CNTR	24/12
1			1

CIRCUIT DESCRIPTION

TPS is used to select the reference signal output waveform, 1 Hz is outputted when it is "1", and 1024Hz is outputted when it is "0", Since 1Hz output is selected this time, it is stuck at "1".

30ADJ is used to carry out ±30-second adjustment, and ±30-second adjustment is carried out when it is stuck at "1". The operation gets at the ordinary mode when it is stuck at "0".

CNTR is used to reset the counter. The operation gets in the reset mode when it is stuck at "1", and after that the content of the specified counter is reset. The operation gets at the ordinary mode when it is stuck at "0".

24/12 is used to switch the display mode. The 24-hour display mode is selected when it is stuck at "1", and the 12-hour display mode is selected when it is stuck at "0".

This time it is stuck at "1", because the 24-hour display mode is selected.

- **CONTROL REGISTER 2**

This is the flat used to detect the state when the operation is in the clock mode.

CONTROL REGISTER 2 (CNT2, 1110)

D3	D2	D1	D0
STA	DET	0	0

STA is used to check the end-around carry of the time and the calendar. It is stuck at "1" when end-around carry is in progress, and at "0" when there is no end-around carrry.

DET is used to check the power ON clear detection. It is stuck at "1" when power ON clear is detected, and at "0" in the ordinary mode.

LIST OF TERMINALS OF THE PARALLEL→SERIAL CONVERTER IC (PARALLEL IN, SERIAL OUT) CONTROL UNIT (X53-346X-XX)

8-bit Shift Register (HD74HC165F): IC7

Terminal No.	Name	Function	I/O Expander terminal name
1	S/L	Data shift/load selection terminal S/L= "L": Data entered in the 8 inputs (A to H) are stored in the various registers, asynchronously with the clock. S/L= "H": Successive shift operations are carried out at the leading edge of the various flip-flops.	PB5
2	CLOCK	Data shift synchronization signal input terminal	PB1
14	D (P_B3)	Parallel input terminal (bit 3). Destination data (bit 3) 0: Destination bit "0" 1: Destination bit "1"	
13	C (P_B2)	Parallel input terminal (bit 2). Destination data (bit 2) 0: Destination bit "0" 1: Destination bit "1"	
12	B (P_B1)	Parallel input terminal (bit 1). Destination data (bit 1) 0: Destination bit "0" 1: Destination bit "1"	
11	A (P_B0)	Parallel input terminal (bit 0). Destination data (bit 0) 0: Destination bit "0" 1: Destination bit "1"	
9	QH	Serial data output terminal	PC3
10	SI	Serial data input terminal	
6	H (P_RPT)	Parallel input terminal (bit 7). Existence of repeater function 0: No repeater function 1: Repeater function	
5	G (P_FANDL I)	Parallel input terminal (bit 6). FAN delay time setting (bit 1) *1 The time is set in combination with terminal No.4.	

CIRCUIT DESCRIPTION

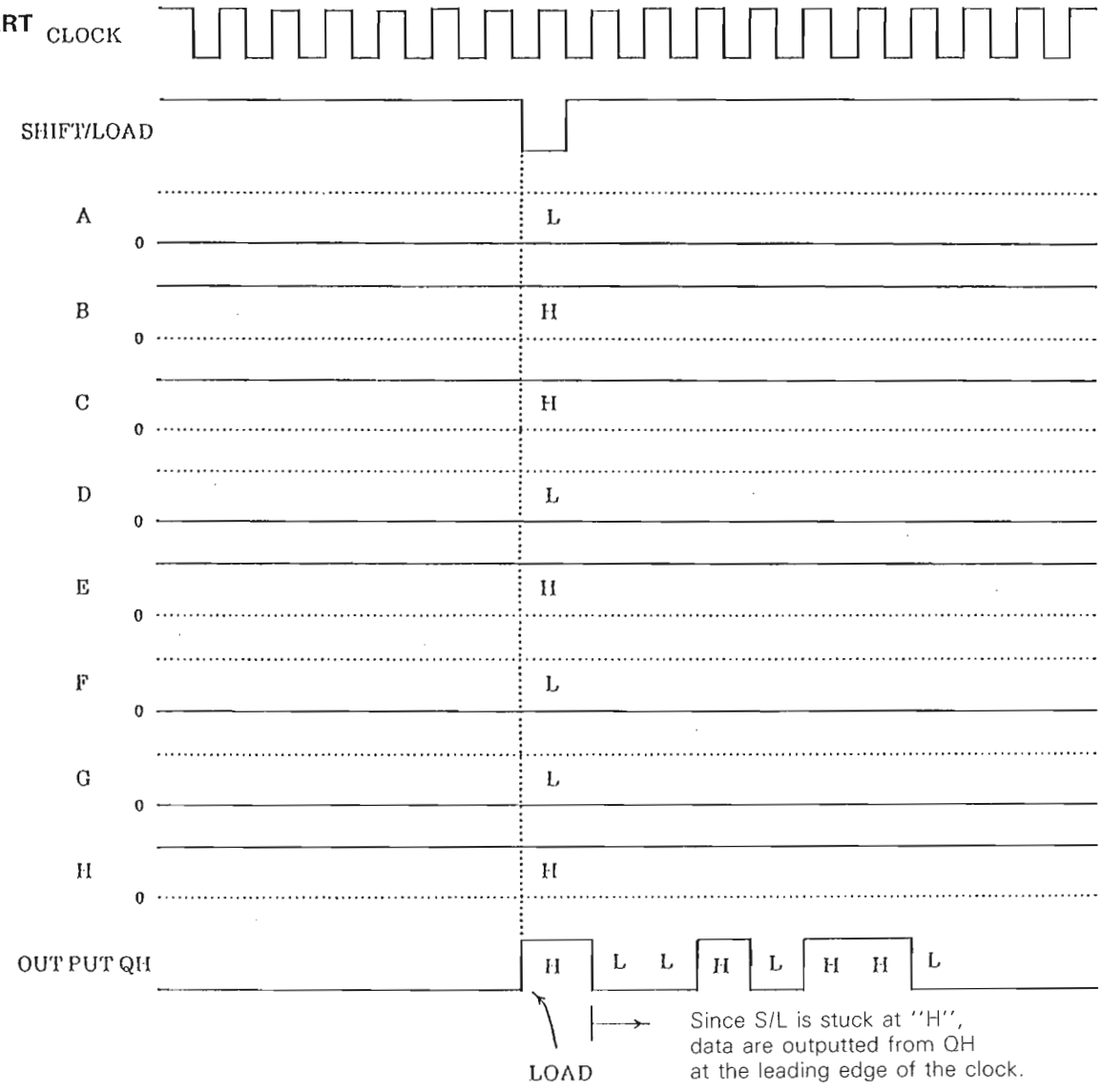
8-bit Shift Register (HD74HC165F): IC7

Terminal No.	Name	Function	I/O Expander terminal name
4	F (P_FANDL0)	Parallel inptu terminal (bit 5). FAN delay time setting (bit 0) *1 The time is set in combination with terminal No.5.	
3	E (P_MDFY)	Parallel input terminal (bit 4). Transmission remodeling data (bit 4) 0: Remodeling 1: No remodeling	

*1 FAN Delay Time setting input

FAN control	P_FANDL 1	P_FANDL 0
Permanently ON when POWER is ON	0	0
ON during transmission	0	1
ON during transmission +ON during 1 minute after and of transmission	1	0
ON during transmission +ON during 2 minutes after end of transmission	1	1

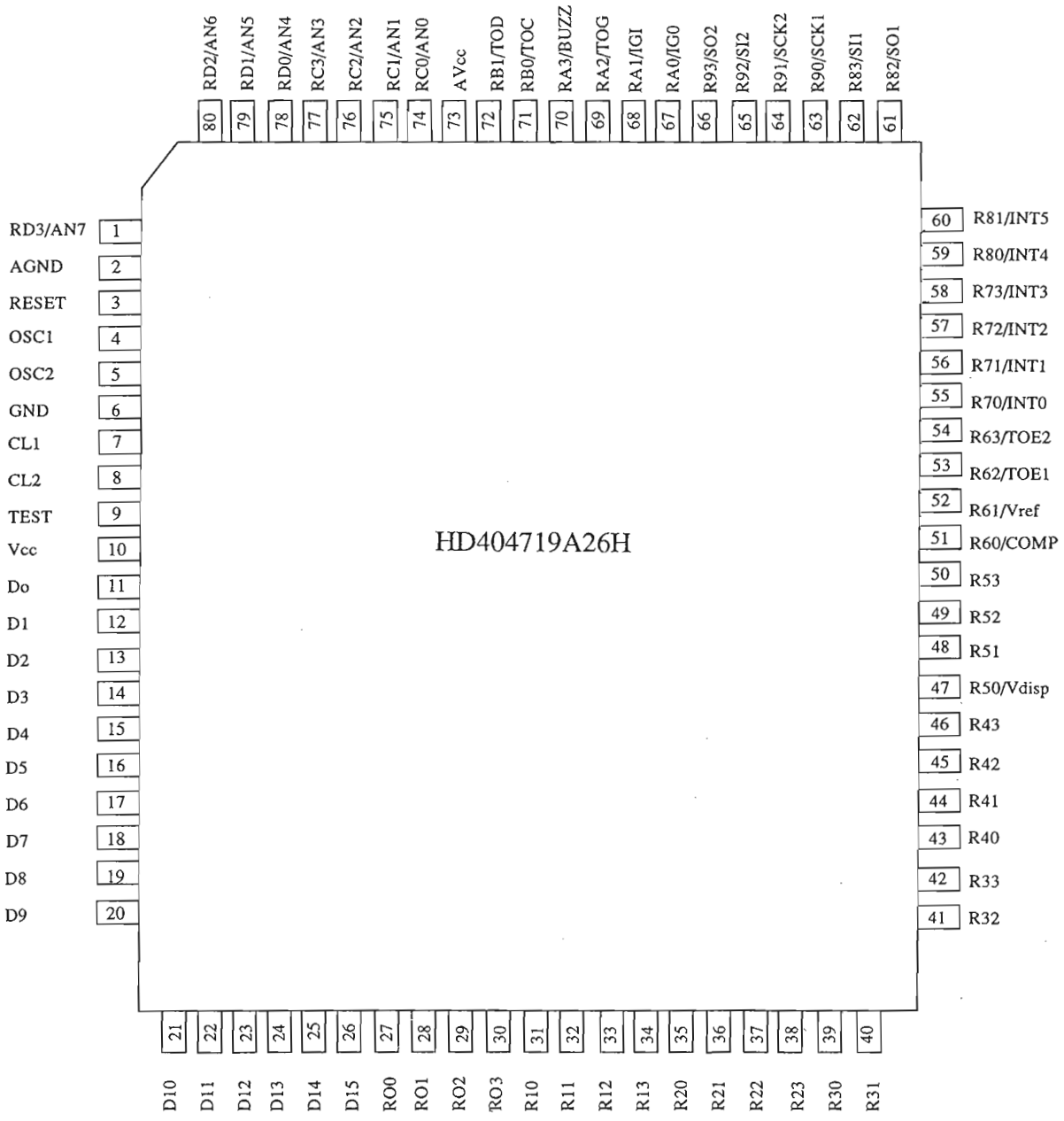
• **TIMING CHART**



CIRCUIT DESCRIPTION

I/O PORT SPECIFICATION LIST

DISPLAY UNIT (X54-3130-11): IC1 (HD404719A26H)



CIRCUIT DESCRIPTION

HD404719A26H I/O PORT LIST: IC1

PIN NO.	μ COM Port	Port name	I/O		Pull Up	Content
			PS ON	PS OFF		
1	RD_3/AN_7		I	I		GND (DONT USE)
2	AGND					GND
3	RESET		I	I	○ 5 M	RESET
4	OSC_1		I	I		4 MHz Xtal ①
5	OSC_2		O	O		4 MHx Xtal ②
6	GND					GND
7	CL_1		I	I		NC (V_{cc})
8	CL_2		O	O		NC (OPEN)
9	*TEST		I	I		5 V (5M)
10	V_{cc}					5 V (5M)
11	D_0	PD0PSW	I	I		PSW L: ON
12	D_1	PD0VFO	I	I		VFO
13	D_2	PD0MR	I	I		MR
14	D_3	PD0CALL	I	I		CALL
15	D_4	PD0F	I	I		F
16	D_5	PD0BELL	I	I		BELL
17	D_6	PD0TONE	I	I		TONE
18	D_7	PD0REV	I	I		REV
19	D_8	PD0DTSS	I	I		DTSS
20	D_9	PD0LOW	I	I		LOW
21	D_{10}	PD0MUTE	I	I		MUTE
22	D_{11}	PD0LINK	I	I		RC
23	D_{12}	PD0MHZ	I	I		MHz
24	D_{13}	PD0CSA	I	I		C SEL A
25	D_{14}	PD0CSB	I	I		C SEL B
26	D_{15}	PD0CSC	I	I		C SEL C
27	RO_0	PD0BSA	I	I		B SEL A
28	RO_1	PD0BSB	I	I		B SEL B
29	RO_2	PD0BSC	I	I		B SEL C

CIRCUIT DESCRIPTION

HD404719A26H I/O PORT LIST: IC1

PIN NO.	μ COM Port	Port name	I/O		Pull Up	Content
			PS ON	PS OFF		
30	RO3/AN7		I	I		NC (Vcc)
31	RIo		O	O(L)		CS LED A GRN ① *I
32	RI1		O	O(L)		CS LED A GRN ② *I
33	RI2		O	O(L)		CS LED A RED ① *I
34	RI3		O	O(L)		CS LED A RED ② *I
35	R2o		O	O(L)		CS LED B GRN ① *I
36	R21		O	O(L)		CS LED B GRN ② *I
37	R22		O	O(L)		CS LED B RED ① *I
38	R23		O	O(L)		CS LED B RED ② *I
39	R3o		O	O(L)		CS LED C GRN ① *I
40	R31		O	O(L)		CS LED C GRN ② *I
41	R32		O	O(L)		CS LED C RED ① *I
42	R33		O	O(L)		CS LED C RED ② *I
43	R4o		O	O(L)		Function LED L: ON H: OFF
44	R41		O	O(L)		NC (OPEN)
45	R42		—	O(L)		NC (Vcc)
46	R43		—	O(L)		NC (Vcc)
47	R5o/Vdisp		I	I		NC (GND)
48	R51		I	I		NC (GND)
49	R52		I	I		NC (GND)
50	R53		I	I		NC (GND)
51	R6o/COMP		O	I		DISPLAY CK
52	R61/Vref		O	I		DISPALY DT
53	R62/TOE1		O	I		NC (OPEN)
54	R63/TOE2		O	I		NC (OPEN)
55	R7o/*INTo		I	I		SI INT (↘Interruption)
56	R71/*INT1		I	I	PULL DOWN	PS (↗Interruption)
57	R72/*INT2		I	I		ENCODERDT

CIRCUIT DESCRIPTION

HD404719A26H I/O PORT LIST

PIN NO.	μ COM Port	Port name	I/O		Pull Up	Content
			PS ON	PS OFF		
58	R73/*INT3		I	I		ENCODERCK (↖ ↘ Interruption)
59	R80/*INT4		I	I		NC (GND)
60	R81/*INT5		I	I		NC (GND)
61	R82/SO1		O	O(H)		SO
62	R83/SI1		I	I		SI
63	R90/*SCK1		I	I		SCK
64	R91/*SCK2		I	I		NC (GND)
65	R92/SI2		I	I		NC (GND)
66	R93/SO2		I	I		NC (GND)
67	RA0/ICT0		O	O(H)		CLK OUT
68	RA1/ICT1		I	I		NC (GND)
69	RA2/TOG		I	I		NC (GND)
70	RA3/BUZZ		I	I		NC (GND)
71	RB0/TOC		I	I		NC (GND)
72	RB1/TOB		I	I		NC (GND)
73	AVcc					5 V (5 C)
74	RC0/AN0		I	I		VOL A
75	RC1/AN1		I	I		VOL B
76	RC2/AN2		I	I		VOL C
77	RC3/AN3		I	I		SQL A
78	RD0/AN4		I	I		SQL B
79	RD1/AN5		I	I		SQL C
80	RD2/AN6		I	I		B VOLTAGE

○: Pull-up with the hardware
*: LOW active
*1: DIMMER control of the various LED of CSEL is carried out means of 2 ports. THe brightness is shown below.

Port	OFF	Dark	Bright
①	H	L	L
②	H	H	L

CIRCUIT DESCRIPTION

LCD DRIVER (MSM5265) LIST
DISPLAY UNIT (X54-3130-11): IC201 No. 1

IC Pin No.	IC Pin Name	LCD SEG. COM1	LCD SEG. COM2	LCD Term. No.
				COM1
				COM2
30	S80	Ⓐ INPHON	Ⓐ REMOTO	1
29	S79	Ⓐ ON	Ⓐ TIMER	2
28	S78	Ⓐ OFF	Ⓐ ALRM	3
27	S77	Ⓐ TOT	Ⓐ ABC	4
26	S76	Ⓐ MUTE	Ⓐ APO	5
				6
25	S75	Ⓐ S7	Ⓐ S5	7
24	S74	Ⓐ ON AIR	Ⓐ BUSY	8
23	S73	Ⓐ L	Ⓐ SI	9
22	S72	Ⓐ M	Ⓐ S2	10
21	S71	Ⓐ 1-5-9	Ⓐ S3	11
20	S70	Ⓐ S6	Ⓐ S4	12
19	S69		Ⓐ BELL	13
18	S68	Ⓐ <	Ⓐ ALT	14
17	S67		Ⓐ IGbc	15
16	S66	Ⓐ L-	Ⓐ R-	16
15	S65	Ⓐ 100Ma	Ⓐ 100Mf	17
14	S64	Ⓐ 100Md	Ⓐ 100Me	18
13	S63	Ⓐ 100Mc		19
12	S62	Ⓐ 100Mb	Ⓐ 100Mg	20
11	S61	Ⓐ CONT	Ⓐ PTT	21
10	S60	Ⓐ 10Ma	Ⓐ 10Mf	22
9	S59	Ⓐ 10Md	Ⓐ 10Me	23
8	S58	Ⓐ 10Mc		24
7	S57	Ⓐ 10Mb	Ⓐ 10 Mg	25
6	S56	Ⓐ >	Ⓐ +	26
5	S55	Ⓐ T	Ⓐ C CSS	27

No. 2

IC Pin No.	IC Pin Name	LCD SEG. COM1	LCD SEG. COM2	LCD Term. No.
4	S54	Ⓐ IMa	Ⓐ IMf	28
3	S53	Ⓐ IMd	Ⓐ IMe	29
2	S52	Ⓐ IMc	Ⓐ IMdp	30
1	S51	Ⓐ IMb	Ⓐ IMg	31
100	S50	Ⓐ DTSS	Ⓐ REV	32
99	S49	Ⓐ 100Ka	Ⓐ 100Kf	33
98	S48	Ⓐ 100Kd	Ⓐ 100Ke	34
97	S47	Ⓐ 100Kc		35
96	S46	Ⓐ CLKdp	Ⓐ 100Kdp	36
95	S45	Ⓐ 100Kb	Ⓐ 100Kg	37
94	S44	Ⓐ Burst1	Ⓐ Burst2	38
93	S43	Ⓐ 10Ka	Ⓐ 10Kf	39
92	S42	Ⓐ 10Kd	Ⓐ 10Ke	40
91	S41	Ⓐ 10Kc	Ⓐ 10Kdp	41
90	S40	Ⓐ 10Kb	Ⓐ 10Kg	42
89	S39	Ⓐ ☆	Ⓐ F	43
88	S38	Ⓐ 1Ka	Ⓐ 1Kf	44
87	S37	Ⓐ 1Kd	Ⓐ 1Ke	45
86	S36	Ⓐ 1Kc	Ⓐ 05 K	46
85	S35	Ⓐ 1Kb	Ⓐ 1Kg	47
84	S34	Ⓐ +U	Ⓐ CO	48
83	S33	Ⓐ MRHa	Ⓐ MRHf	49
82	S32	Ⓐ MRHd	Ⓐ MRHe	50
81	S31	Ⓐ MRHc	Ⓐ LOCK	51
80	S30	Ⓐ MRHb	Ⓐ MRHg	52
79	S29	Ⓐ MRLa	Ⓐ MRLf	53
78	S28	Ⓐ MRLd	Ⓐ MRLe	54
77	S27	Ⓐ MRLc		55
76	S26	Ⓐ MRLb	Ⓐ MRLg	56
				57

CIRCUIT DESCRIPTION

No. 3

IC Pin No.	IC Pin Name	LCD SEG. COM1	LCD SEG. COM2	LCD Term.No.
75	S25	Ⓑ S7	Ⓑ S5	58
74	S24	Ⓑ ONAIR	Ⓑ BUSY	59
73	S23	Ⓑ L	Ⓑ SI	60
72	S22	Ⓑ M	Ⓑ S2	61
71	S21	Ⓑ 1-5-9	Ⓑ S3	62
70	S20	Ⓑ S6	Ⓑ S4	63
69	S19		Ⓑ BELL	64
68	S18	Ⓑ <	Ⓑ ALT	65
67	S17	Ⓑ IGa	Ⓑ IGf	66
66	S16	Ⓑ IGd	Ⓑ IGe	67
65	S15	Ⓑ IGc		68
64	S14	Ⓑ IGb	Ⓑ IGg	69
63	S13	Ⓑ L-	Ⓑ R-	70
62	S12	Ⓑ 100Ma	Ⓑ 100Mf	71
61	S11	Ⓑ 100Md	Ⓑ 100Me	72
60	S10	Ⓑ 100Mc		73
59	S9	Ⓑ 100Mb	Ⓑ 100Mg	74
58	S8	Ⓑ CONT	Ⓑ PTT	75
57	S7	Ⓑ 10Ma	Ⓑ 10Mf	76
56	S6	Ⓑ 10Md	Ⓑ 10Me	77
55	S5	Ⓑ 10Mc		78
54	S4	Ⓑ 10Mb	Ⓑ 10Mg	79
53	S3	Ⓑ >	Ⓑ +	80
52	S2	Ⓑ T	Ⓑ C CSs	81
51	S1	Ⓑ IMa	Ⓑ IMf	82
48	COM-A			
49	COM-B			

DISPLAY UNIT (X54-3130-11): IC202 No. 1

IC Pin No.	IC Pin Name	LCD SEG. COM1	LCD SEG. COM2	LCD Term.No.
				COM1
				COM2
30	S80	Ⓑ IMd	Ⓑ IMe	83
29	S79	Ⓑ IMc	Ⓑ IMdp	84
28	S78	Ⓑ IMb	Ⓑ IMg	85
27	S77	Ⓑ DTSS	Ⓑ REV	86
26	S76	Ⓑ 100Ka	Ⓑ 100Kf	87
25	S75	Ⓑ 100Kd	Ⓑ 100Ke	88
24	S74	Ⓑ 100Kc	Ⓑ 100Kdp	89
23	S73	Ⓑ CLKdp		90
22	S72	Ⓑ 100Kb	Ⓑ 100Kg	91
21	S71	Ⓑ Burst1	Ⓑ Burst2	92
20	S70	Ⓑ 10Ka	Ⓑ 10Kf	93
19	S69	Ⓑ 10Kd	Ⓑ 10Ke	94
18	S68	Ⓑ 10Kc	Ⓑ 10Kdp	95
17	S67	Ⓑ 10Kb	Ⓑ 10Kg	96
16	S66	Ⓑ ☆	Ⓑ F	97
15	S65	Ⓑ 1Ka	Ⓑ 1Kf	98
14	S64	Ⓑ 1Kd	Ⓑ 1Ke	99
13	S63	Ⓑ IKc	Ⓑ 05K	100
12	S62	Ⓑ 1Kb	Ⓑ 1Kg	101
11	S61	Ⓑ +U	Ⓑ CO	102
10	S60	Ⓑ MRHa	Ⓑ MRHf	103
9	S59	Ⓑ MRHd	Ⓑ MRHe	104
8	S58	Ⓑ MRHc	Ⓑ LOCK	105
7	S57	Ⓑ MRHb	Ⓑ MRHg	106
6	S56	Ⓑ MRLa	Ⓑ MRLf	107
5	S55	Ⓑ MRLd	Ⓑ MRLe	108

CIRCUIT DESCRIPTION

DISPLAY UNIT (X54-3130-11): IC202 No. 2

IC Pin No.	IC Pin Name	LCD SEG. COM1	LCD SEG. COM2	LCD Term. No.
4	S54	Ⓑ MRLc		109
3	S53	Ⓑ MRLb	Ⓑ MRLg	110
				111
2	S52	Ⓒ S7	Ⓒ S5	112
1	S51	Ⓒ ONAIR	Ⓒ BUSY	113
100	S50	Ⓒ L	Ⓒ S1	114
99	S49	Ⓒ M	Ⓒ S2	115
98	S48	Ⓒ 1-5-9	Ⓒ S3	116
97	S47	Ⓒ S6	Ⓒ S4	117
96	S46		Ⓒ BELL	118
95	S45	Ⓒ <	Ⓒ ALT	119
94	S44		Ⓒ 1Gbc	120
93	S43	Ⓒ L-	Ⓒ R-	121
92	S42	Ⓒ 100Ma	Ⓒ 100Mf	122
91	S41	Ⓒ 100Md	Ⓒ 100Me	123
90	S40	Ⓒ 100Mc		124
89	S39	Ⓒ 100Mb	Ⓒ 100Mg	125
88	S38	Ⓒ CONT	Ⓒ PTT	126
87	S37	Ⓒ 10Ma	Ⓒ 10Mf	127
86	S36	Ⓒ 10Md	Ⓒ 10Me	128
85	S35	Ⓒ 10Mc		129
84	S34	Ⓒ 10Mb	Ⓒ 10Mg	130
83	S33	Ⓒ >	Ⓒ +	131
82	S32	Ⓒ T	Ⓒ C CSS	132
81	S31	Ⓒ 1Ma	Ⓒ 1Mf	133
80	S30	Ⓒ 1Md	Ⓒ 1Me	134
79	S29	Ⓒ 1Mc	Ⓒ 1Mdp	135
78	S28	Ⓒ 1Mb	Ⓒ 1Mg	136
77	S27	Ⓒ DTS	Ⓒ REV	137
76	S26	Ⓒ 100Ka	Ⓒ 100Kf	138

No. 3

IC Pin No.	IC Pin Name	LCD SEG. COM1	LCD SEG. COM2	LCD Term. No.
75	S25	Ⓒ 100Kb	Ⓒ 100Ke	139
74	S24	Ⓒ 100Kc	Ⓒ 100Kdp	140
73	S23	Ⓒ CLKdp		141
72	S22	Ⓒ 100Kb	Ⓒ 100Kg	142
71	S21	Ⓒ Burst1	Ⓒ Burst2	143
70	S20	Ⓒ 10Ka	Ⓒ 10Kf	144
69	S19	Ⓒ 10Kd	Ⓒ 10Ke	145
68	S18	Ⓒ 10Kc	Ⓒ 10Kdp	146
67	S17	Ⓒ 10Kb	Ⓒ 10Kg	147
66	S16	Ⓒ ☆	Ⓒ F	148
65	S15	Ⓒ 1Ka	Ⓒ 1Kf	149
64	S14	Ⓒ 1Kd	Ⓒ 1Ke	150
63	S13	Ⓒ 1Kc	Ⓒ 05K	151
62	S12	Ⓒ 1Kb	Ⓒ 1Kg	152
61	S11	Ⓒ +U	Ⓒ CO	153
60	S10	Ⓒ MRHa	Ⓒ MRHf	154
59	S9	Ⓒ MRHd	Ⓒ MRHe	155
58	S8	Ⓒ MRHc	Ⓒ LOCK	156
57	S7	Ⓒ MRHb	Ⓒ MRHg	157
56	S6	Ⓒ MRLa	Ⓒ MRLf	158
55	S5	Ⓒ MRLd	Ⓒ MRLe	159
54	S4	Ⓒ MRLc		160
53	S3	Ⓒ MRLb	Ⓒ MRLg	161
52	S2			
51	S1			
48	COM-A			
49	COM-B			

CIRCUIT DESCRIPTION

• TONE OUTPUT

The TONE output is obtained by outputting, from CPU, the pulse corresponding to the preset tone, and by filtering it. (Figure 41)

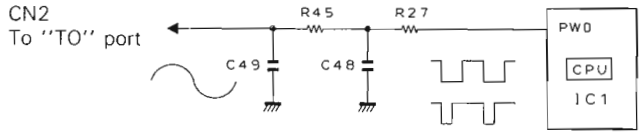


Fig. 41

• INPUT/OUTPUT OF CTCSS (OPTION TSU-7)

Data to the CTDSS unit is outputted by P80, P47 and P43. Moreover, since P80 has also the function of checking the connection it becomes an input when the power is turned ON, and after checking the connection it becomes an output. CTCSS does not turn ON when there is no connection. Figure 42 shows the data transmission format, and Figure 44 shows the data configuration. The "L" level, obtained when the tone is detected from the CTCSS unit and its coincidence is confirmed, is entered in P81 of the microprocessor, and then the squelch is opened.

Each CTCSS unit is able to cope with 3 bands. This operation is executed by switching the low frequency signal outputted by the band unit. (Figure 43).

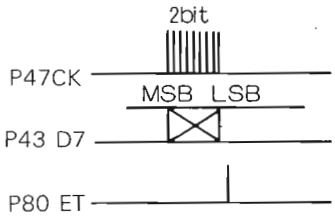


Fig. 42 CTCSS Data Transfer Format

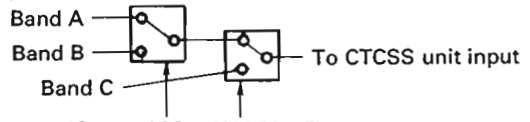


Fig. 43

Tone frequency selection data of CTCSS FX365

	D0	D1	D2	D3	D4	D5
Example 88.5 Hz (DTMF unit)	L	H	H	H	L	L

Fig. 44 CTCSS Data Configuration

• INPUT/OUTPUT OF DTMF

Data to DTMF is outputted by P66, 67 and P60 to P63 of the microprocessor.

P60 to P63 are the data in the case of the encoder, and tones corresponding to each data are outputted from the TONE terminal) of IC10 (TCD35219F) while P66 is stuck at "H".

As for the decoder, the detected signals corresponding to each band are switched at IC108, 109, in the same way as in CTCSS, and after that it passes through the analog switch IC8 and is entered in the DTMF decoder IC11 (LC7385M). When an effective tone is detected, the terminal STD is stuck at "H", and P67 of the microprocessor is enabled. As a result, data are entered in P60 to P63, and the coincidence with the preset DTSS codes is checked by the microcomputer.

On the other hand, the input from the DTMF microphone is read and controlled by switching the input of IC11 by means of Q7 and the microprocessor. The ports of IC11 are shown in the following table.

• PLL data output

The PLL data is passed through I/O expander IC101 (CXD 1095Q) from the microcomputer and output to each band unit with EP, CK, and DT signals and three serial data items.

A PLL IC (M56760FP) is used in common with the 144 and 430 TX/RX units. Figure 45 shows the data configuration. Figure 46 and 47 shows the PLL data transfer format.

LIST OF PORTS OF IC11: LC7385M

Pin No.	Name	I/O	Function description
1	IN^+	I	Non-inverted input of the input amplifier
2	IN^-	I	Inverted input of the input amplifier
3	GS	O	Output of the output amplifier
4	V_{REF}	O	Reference voltage output of Voo/2
5	B/H	I	Selects the output format of Q1 to Q4. Binary (2 of 8) code when stuck at "H". Hexadecimal code when stuck at "L".
6	PD	I	Operation switched to pweor down mode when stuck at "H".
7	OSC1	I	An osciallator circuit is composed by connecting a 3 569545MHz quartz oscillator between these terminals.
8	OSC2	O	
9	Vss		Power supply terminal, normally 0V
10	TOE	I	Controls the 3 state output of Q1 to Q4. Enabled when stuck at "H". High impedance when stuck at "L".
11	Q_1	O	3 state received data output
12	Q_2		
13	Q_3		
14	Q_4		
15	StD	O	Stuck at "H" when the connection time of the effective tone pari esceeds the preset time preset by the add-on CR.
16	ESt	O	Stuck at "H" when the effective tone pari is detected.
17	St/GT	I/O	The guard time is preset by connecting CR.
18	Voo		Power supply terminal. Normally 5V.

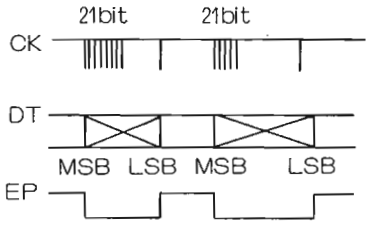
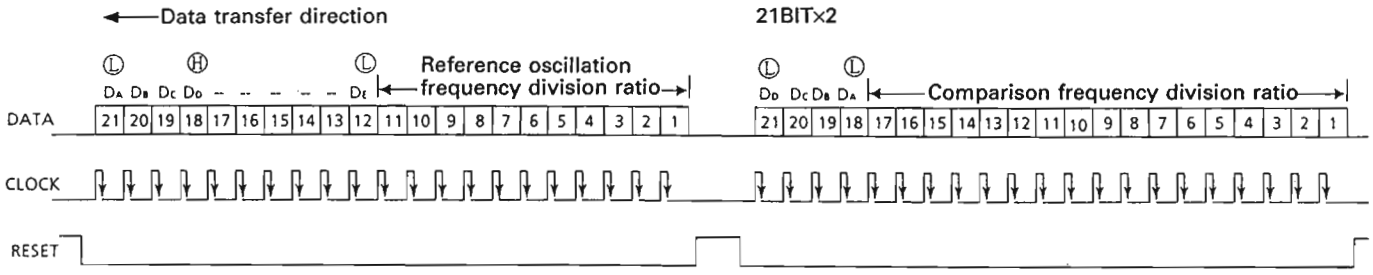


Fig. 45 PLL Data Configuration

CIRCUIT DESCRIPTION



f_{REF} = 12800 ÷ (8 x Reference oscillation frequency division ratio)

Reference oscillation frequency division ratio = 16000 / f_{REF} (kHz)

5 kHz ..... P = 320
6.25 kHz ..... P = 256

Reference oscillation frequency division ratio

1	2	3	4	5	6	7	8	9	10	11	
0	0	0	0	0	0	1	0	1	0	0	(320)
0	0	0	0	0	0	0	0	1	0	0	(256)

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	01 40 5 kHz
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	01 00 5.25 kHz

Special bit function

Bit	Name	H	L
D_A	Data latch selection	Reference	Comparison
D_B	SW2	H: OFF	L: ON
D_C	SW1	H: OFF	L: ON
D_D	POWER switch	OFF	ON
D_E	Test	Test	Normal

PLL data-to-bit relationship

ADD	BIT			
	0	1	2	3
1BH	1	2	3	4
1CH	5	6	7	8
1DH	9	10	11	12
1BH	13	14	15	16
1FH	17	–	–	–

Fig. 46 M56760 PLL DATA

1F	1E	1D	1C	1B	1A
–	6	10	14	18	1
–	7	11	15	19	2
–	8	12	16	20	3
5	9	13	17	21	4

1F	1E	1D	1C	1B	1A
–	2^{15}	2^{11}	2^7	2^3	D_D
–	2^{14}	2^{10}	2^6	2^2	D_C
–	2^{13}	2^9	2^5	2^1	D_B
2^{16}	2^{12}	2^8	2^4	2^0	D_A

For frequency division ratio setting

1F	1E	1D	1C	1B	1A
–	×	D_E	2^7	2^3	D_D
–	×	2^{10}	2^6	2^2	D_C
–	×	2^9	2^5	2^1	D_B
×	×	2^8	2^4	2^0	D_A

For comparison frequency

Data D_E	State
L	Normal
H	Test

Data D_E	PLL
L	POWER switch ON
H	OFF

Data		Output port	
D_H	D_C	SW2	SW1
L	L	ON	ON
H	L	OFF	ON
L	H	ON	OFF
H	H	OFF	OFF

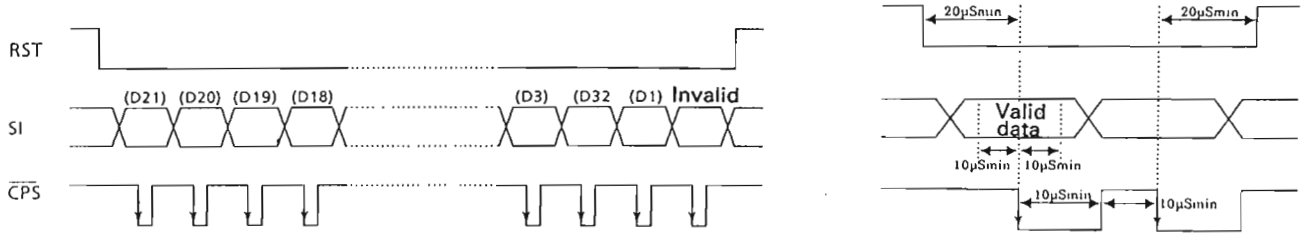


Fig. 47 M56760 PLL DATA OUTPUT

CIRCUIT DESCRIPTION

The PLL and reference frequency-division ratio data input to the 1200 TX/RX unit are output from P21 (CK), P22 (DT), and P23 (EP1) of the CPU. The reference frequency-division ratio data (R) is output only when the power is switched on and when 10 and 12.5 kHz reference frequencies are changed.

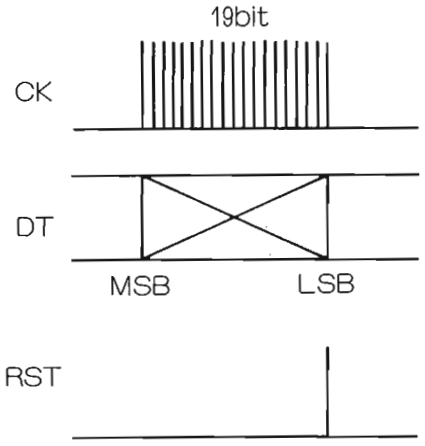


Fig. 48 PLL Frequency-Division Ratio Data Transfer Format

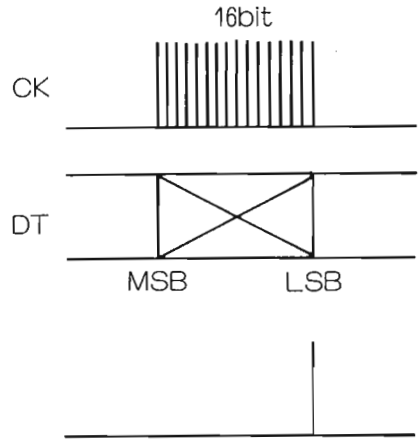


Fig. 49 Reference Frequency-Division Ratio Data Transfer Format

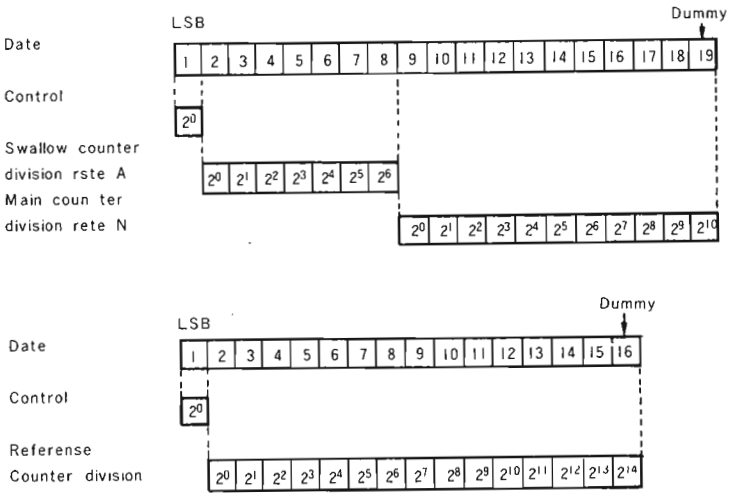


Fig. 50 Data Configuration

CIRCUIT DESCRIPTION

AF SIGNAL SYSTEM

• OUTLINE

Signals coming from the detected signal RA of each band unit pass through the electronic potentiometer, are added at the mute circuit and buzzer circuit, and after passing through the speaker switching circuit they are outputted to the power amplifier and to the speakers.

Each band has an independent AF signal, and any arbitrary combination can be outputted through the speaker, depending on the position where the speaker jack is plugged.

• VOLUME/BUZZER CIRCUIT

The angles of the potentiometers of the various bands, that are located on the panel unit, are transformed to 5 bit data through A/D conversion executed by the microprocessor of the panel unit, and are sent to the microprocessor of the control unit. These data are outputted by the I/O expander: IC101 to IC112(HIC) as serial data.

The buzzer sound heard when the key is pressed is outputted from the IC(P44) of the control unit, MIXed with the DTMF monitor output, and is outputted to IC112.

IC112 carries out the LEVEL/MUTE processing of the audio signal in conformity with the received data, and after that the signal is outputted to the speaker changeover switch: IC106. (Figure 51).

The volume level is set for the speaker output and buzzer sound (''beep'' sound) of each band, by using the 2 electronic potentiometers (MB87032) built into IC112.

The data have 28 bit composition, with 20 bits used to set the level. (The remaining 8 bits are used as commands and other applications).

The data are fetched at the trailing edge of the clock. (Figure 52).

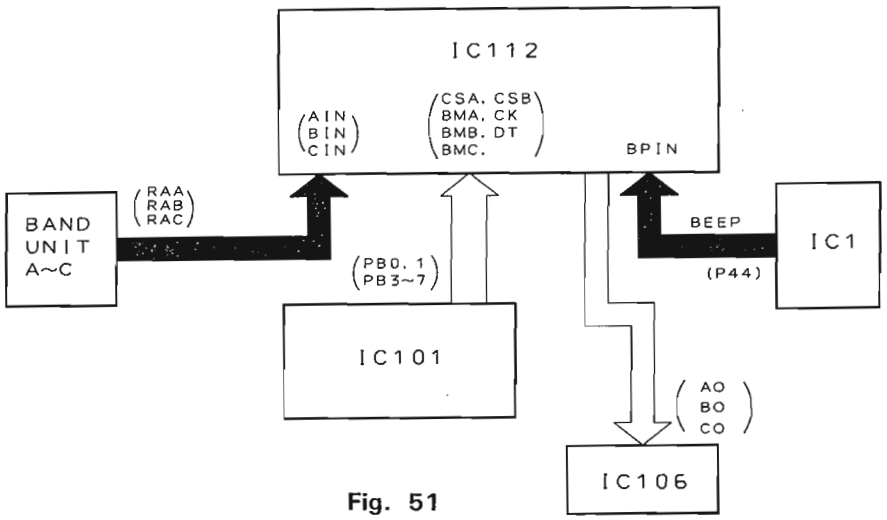


Fig. 51

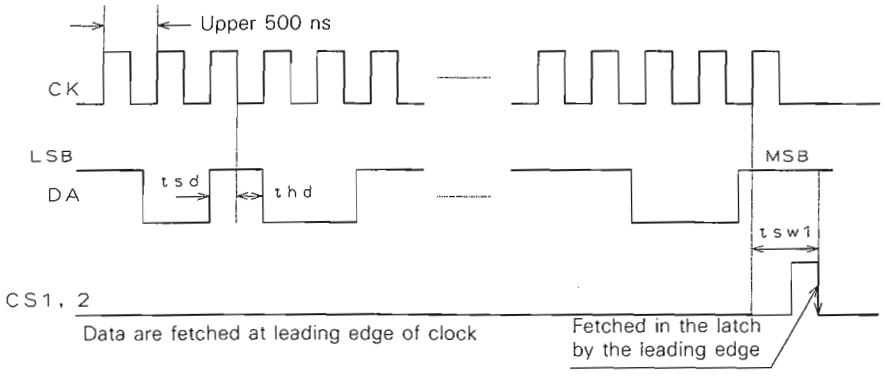


Fig. 52

CIRCUIT DESCRIPTION

• SPEAKER SWITCHING CIRCUIT

Four speaker jacks are provided in total, one in each band unit (rear) and one in the control unit (side).

As for the functions of the various terminals, the speaker jack of the band unit outputs the AF signal of the band in question when the speaker is connected.

The speaker jack of the control unit outputs the signal obtained by mixing the remaining AF signals. This signal is outputted by the internal speaker when there is no speaker connected to the speaker jack, Figure 53 shows the main circuit.

When there is nothing connected to the speaker jack, the signal is entered in the adder of IC103. The level of the adder does not change, irrespective of the number of signals (1 to 3) that are added.

For example, when one wants to mix the signals of speakers A and C of band B and to output the obtained result from the remaining speaker, it is possible to execute this operation by connecting with the jack of band B and the jack of the control unit.

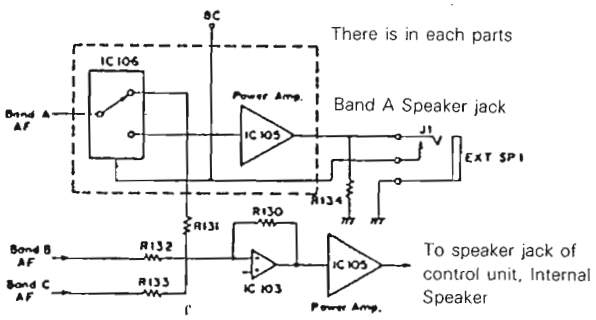


Fig. 53

• SQUELCH CIRCUIT

Squelch can be preset at each band by means of the squelch potentiometer located in the panel unit. The squelch potentiometer signal is converted to 5 bit data through A/D conversion at the microprocessor of the panel unit.

Data are sent from the panel unit to the microprocessor of the control unit, and after data conversion they are sent as serial data from IC101 of the control unit to IC113 (HIC). (Refer to the SHIFT REGISTER section for the logic). D/A conversion is carried out at IC113 through the combination of the shift register and the analog switch, and the control voltage of IC110 is generated by the RDSQ terminal to carry out the control of the RD line. (Figure 54).

The setting of the squelch level turns the analog switch ON/OFF by means of the 5 bit data of the various bands (Refer to the LIST OF PORTS of the shift registers A and B).

Since a resistance is connected between the two terminals of the analog switch, the resistance value is changed by the combination of the ON/OFF states of the switches. The voltage level of the SQ output can be controlled as a result. (Figure 55)

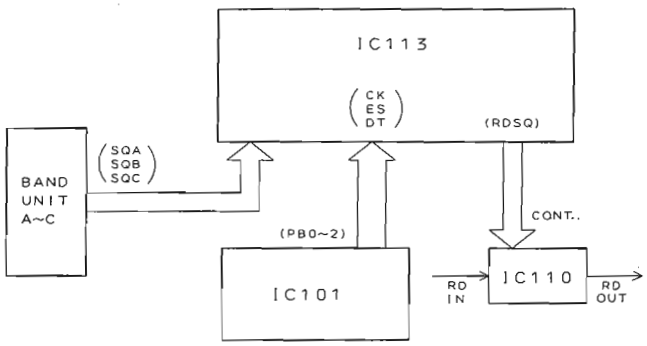


Fig. 54

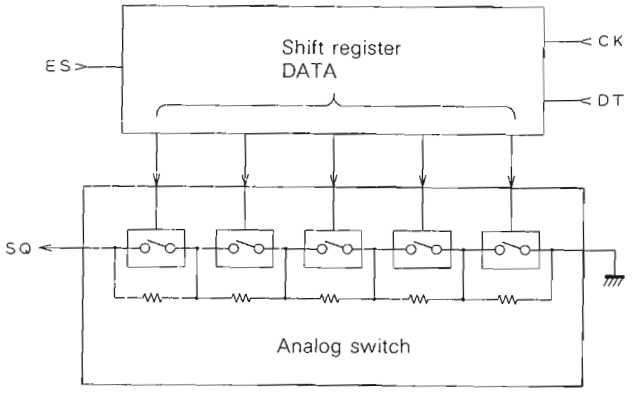


Fig. 55

CIRCUIT DESCRIPTION

Connector Connecting the Band Unit and Control Unit

- **Outline**

The pin assignments of the connector that connects the control unit and band unit are common in three bands. The band unit is also used to check which band unit is connected.

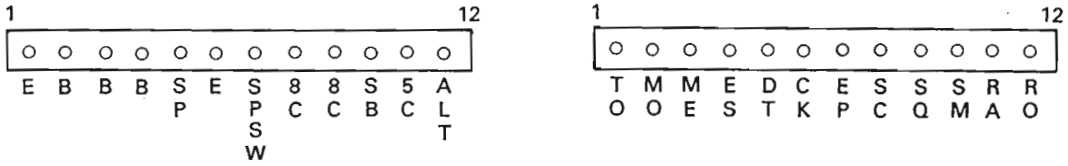


Fig. 56 **Connector Connecting the Band Unit and Control Unit**

Pin No.	Name	Function	Pin No.	Name	Function
1	E	GND	1	TO	67.0 to 250.3 Hz subtone output
2	B	13.8 V input	2	MO	Audio signal from microphone (including DTMF)
3	B		3	ME	Microphone ground
4	B		4	ES	Shift-register enable output
5	SP	AF signal is output when speaker jack is connected.	5	CK	Shift-register PLL clock
6	E	GND	6	DT	Shift-register PLL data
7	SPSW	Speaker jack connection and detection. "H" during connection.	7	EP	PLL enable
8	8C	8 V is output during the power-on sequence.	8	SC	"L" when squelch input is busy.
9	8C		9	SQ	50 k ohms when squelch D/A output is tight.
10	SB	13.8 V is output during the power-on sequence.	10	SM	Signal-strength meter voltage input
11	SC	5 V is output during the power-on sequence.	11	RA	Detection input (squelch circuit)
12	ALT	ALT voltage input	12	RD	Detection input (no squelch circuit)

Table 20 Pin functions (as viewed from the control unit)

- **Band retrieval**

Each band is retrieved through the EP, CK, and DT pins. Data is input for retrieval when the power is switched on and when the memory is cleared. Data is then output again.

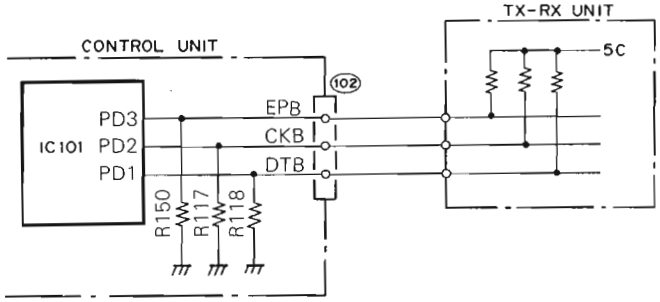


Fig. 57 **Retrieval System**

The control unit is pulled down as shown in Figure 57. Therefore, the DT, CK, and EP pins are set low when no band unit is connected. Pins set high as listed in Table 21 are pulled up when any band unit is connected. The type of connected band unit is then judged.

BAND Unit	DT	CK	EP
No Unit	L	L	L
28	H	L	L
50	H	H	L
144	L	H	H
430	H	L	H
1200	L	L	H

Table 21 Band Retrieval